## *Memory FeRAM*

# 16 K (2 K × 8) Bit I²C

# MB85RC16V

## ■ DESCRIPTION

The MB85RC16V is an FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 2,048 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

Unlike SRAM, the MB85RC16V is able to retain data without using a data backup battery.

The memory cells used in the MB85RC16V have at least $10^{12}$ Read/Write operation endurance per byte, which is a significant improvement over the number of read/write operations than by other nonvolatile memory products.

The MB85RC16V can provide writing in one byte units because the long writing time is not required unlike Flash memory and E²PROM. Therefore, the writing completion waiting sequence like a write busy state is not required.

## ■ FEATURES

- Bit configuration : 2,048 words × 8 bits
- Two-wire serial interface : Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
- Operating frequency : 1 MHz (Max)
- Read/Write endurance : $10^{12}$ times / byte
- Data retention : 10 years ( + 85 °C), 95 years ( + 55 °C), over 200 years ( + 35 °C)
- Operating power supply voltage : 3.0 V to 5.5 V
- Low power consumption : Operating power supply current 90 µA (Typ @1 MHz)
  Standby current 5 µA (Typ)
- Operation ambient temperature range: – 40 °C to + 85 °C
- Package : 8-pin plastic SOP
  RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited. RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

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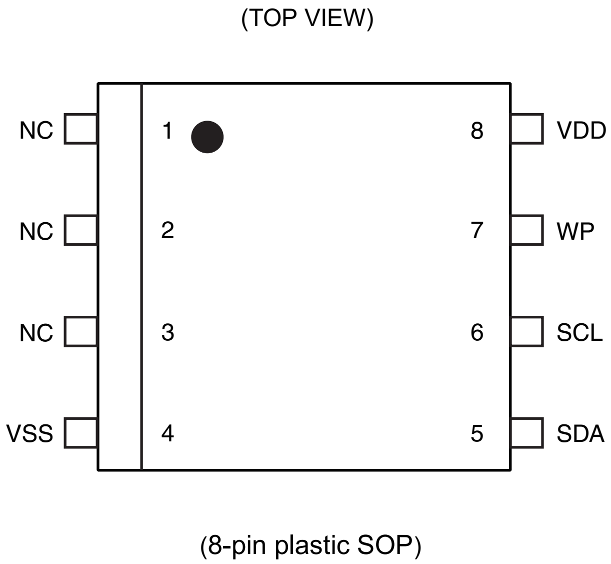
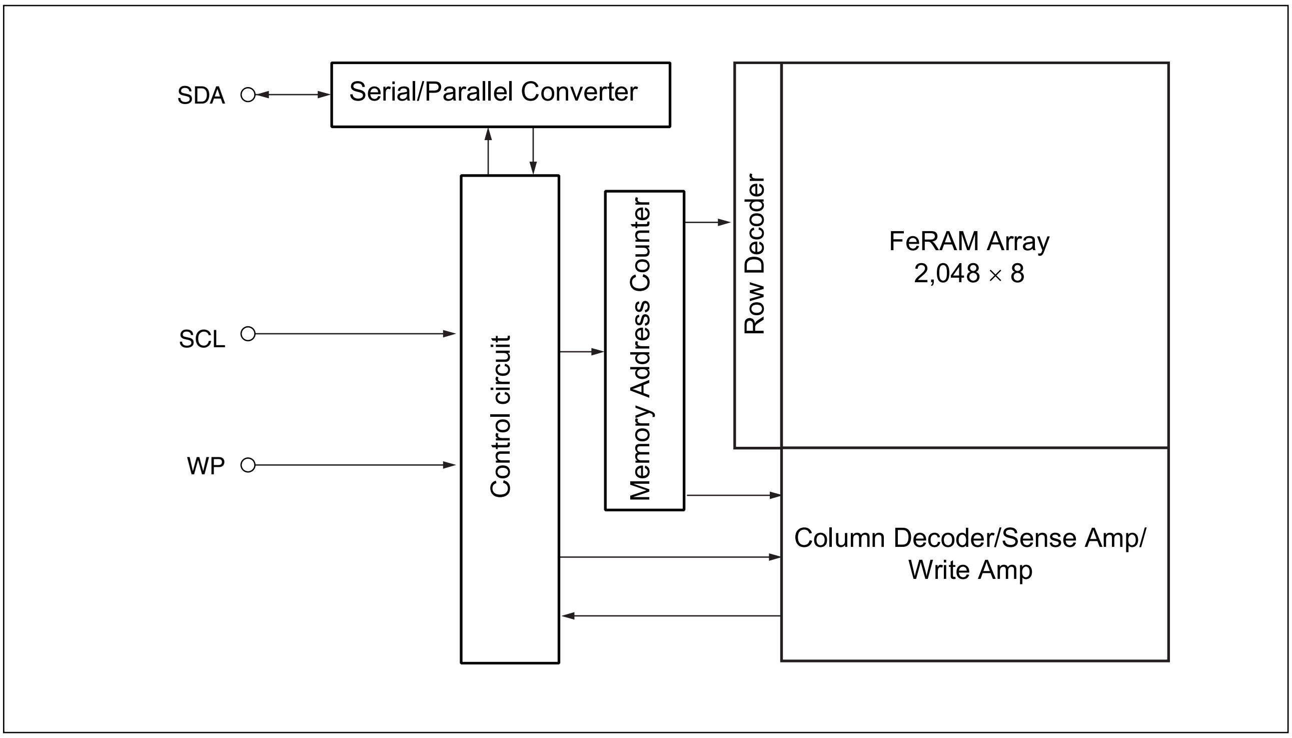
## ■ PIN ASSIGNMENT



## ■ PIN FUNCTIONAL DESCRIPTIONS

| Pin Number | Pin Name | Functional Description |
|---|---|---|
| 1 to 3 | NC | No Connect pins<br>Leave these pins open, or connect to VDD or VSS. |
| 4 | VSS | Ground pin |
| 5 | SDA | Serial Data I/O pin<br>This is an I/O pin which performs bidirectional communication for both memory address and writing/reading data. It is possible to connect multiple devices. It is an open drain output, so a pull-up resistor is required to be connected to the external circuit. |
| 6 | SCL | Serial Clock pin<br>This is a clock input pin for input/output serial data. Data is sampled on the rising edge of the clock and output on the falling edge. |
| 7 | WP | Write Protect pin<br>When the Write Protect pin is the “H” level, writing operation is disabled. When the Write Protect pin is the “L” level, the entire memory region can be overwritten. Reading operation is always enabled regardless of the Write Protect pin input level. The Write Protect pin is internally pulled down to the VSS pin and, that is recognized as the “L” level (write enabled) when the pin is the open state. |
| 8 | VDD | Supply Voltage pin |

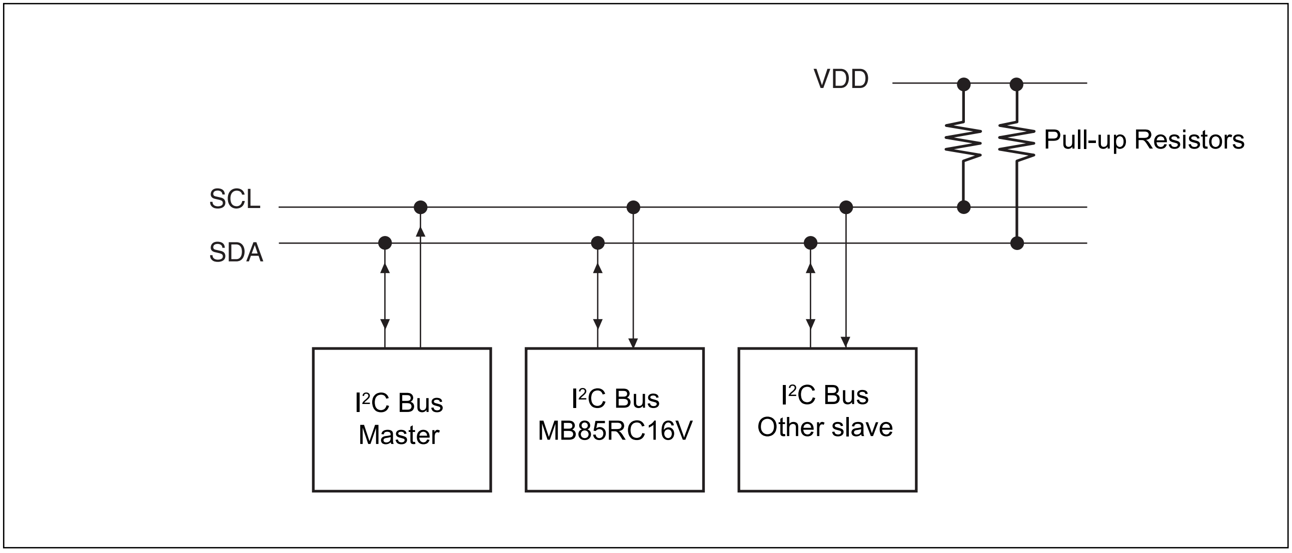
## ■ BLOCK DIAGRAM


SDA
Serial/Parallel Converter
SCL
WP
Control circuit
Memory Address Counter
Row Decoder
FeRAM Array
2,048 × 8
Column Decoder/Sense Amp/
Write Amp

## ■ I²C (Inter-Integrated Circuit)

The MB85RC16V has the two-wire serial interface; the I²C bus,and operates as a slave device.
The I²C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, an I²C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration.

- **I²C Interface System Configuration Example**


VDD
Pull-up Resistors
SCL
SDA
I²C Bus
Master
I²C Bus
MB85RC16V
I²C Bus
Other slave

## ■ I²C COMMUNICATION PROTOCOL

The I²C bus provides communication by two wires only, therefore, the SDA input should change while the SCL is the “L” level. However, when starting and stopping the communication sequence, the SDA is allowed to change while the SCL is the “H” level.

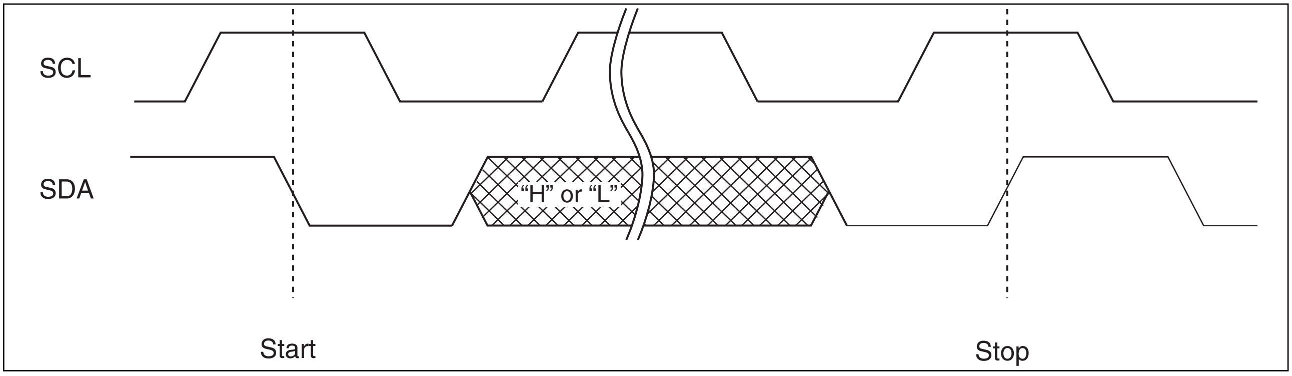
- Start Condition

To start read or write operations by the I²C bus, change the SDA input from the “H” level to the “L” level while the SCL input is in the “H” level.

- Stop Condition

To stop the I²C bus communication, change the SDA input from the “L” level to the “H” level while the SCL input is in the “H” level. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data and enters the standby state.

**• Start Condition, Stop Condition**



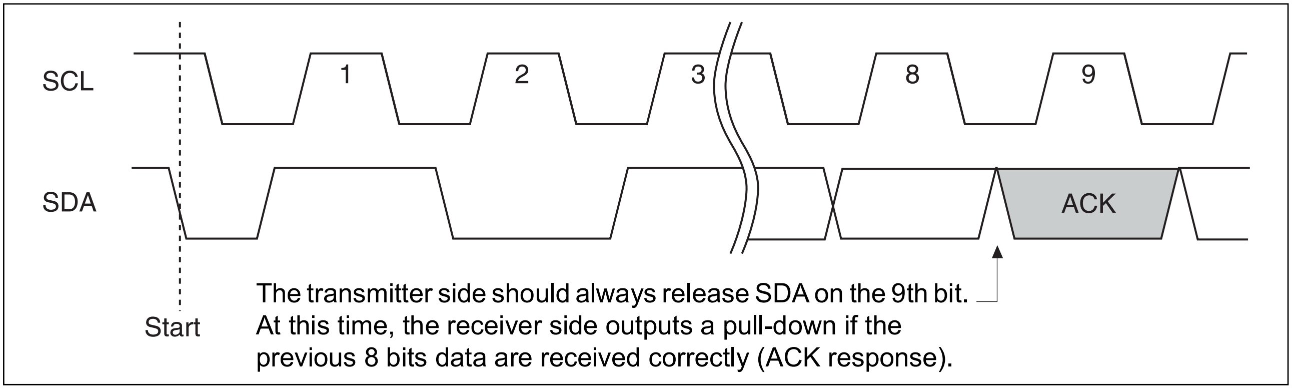
Note : At the write operation, the FeRAM device does not need the programming wait time ($t_{WC}$) after issuing the Stop Condition.

## ■ ACKNOWLEDGE (ACK)

In the I²C bus, serial data including memory address or memory information is sent and received in units of 8 bits. The acknowledge signal indicates that every 8 bits of the data is successfully sent and received. The receiver side usually outputs the “L” level every time on the 9th SCL clock after each 8 bits are successfully transmitted and received. On the transmitter side, the bus is temporarily released to Hi-Z every time on this 9th clock to allow the acknowledge signal to be received and checked. During this Hi-Z released period, the receiver side pulls the SDA line down to indicate the “L” level that the previous 8 bits communication is successfully received.

In case the slave side receives Stop condition before sending or receiving the ACK “L” level, the slave side stops the operation and enters to the standby state. On the other hand, the slave side releases the bus state after sending or receiving the NACK “H” level. The master side generates Stop condition or Start condition in this released bus state.

**• Acknowledge timing overview diagram**



The transmitter side should always release SDA on the 9th bit. At this time, the receiver side outputs a pull-down if the previous 8 bits data are received correctly (ACK response).

## ■ MEMORY ADDRESS STRUCTURE

The MB85RC16V has the memory address buffer to store the 11-bit information for the memory address.

As for byte write, page write and random read commands, the complete 11-bit memory address is configured by inputting the memory upper address (3 bits) and the memory lower address (8 bits), and saved to the memory address buffer. Then access to the memory is performed.

As for a current address read command, the complete 11-bit memory address is configured and saved to the memory address buffer, by inputting the memory upper address (3 bits) and the memory lower address (8 bits) which has saved in the memory address buffer. Then access to the memory is performed.

## ■ DEVICE ADDRESS WORD

Following the start condition, the 8 bit device address word is input. Inputting the device address word decides whether writing or reading operation. However, the clock is always driven by the master. The device address word (8 bits) consists of a device Type code (4 bits), memory upper address code (3 bits), and a Read/Write code (1 bit).

- Device Type Code (4 bits)

The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at “1010” for the MB85RC16V.

- Memory Upper Address Code (3 bits)

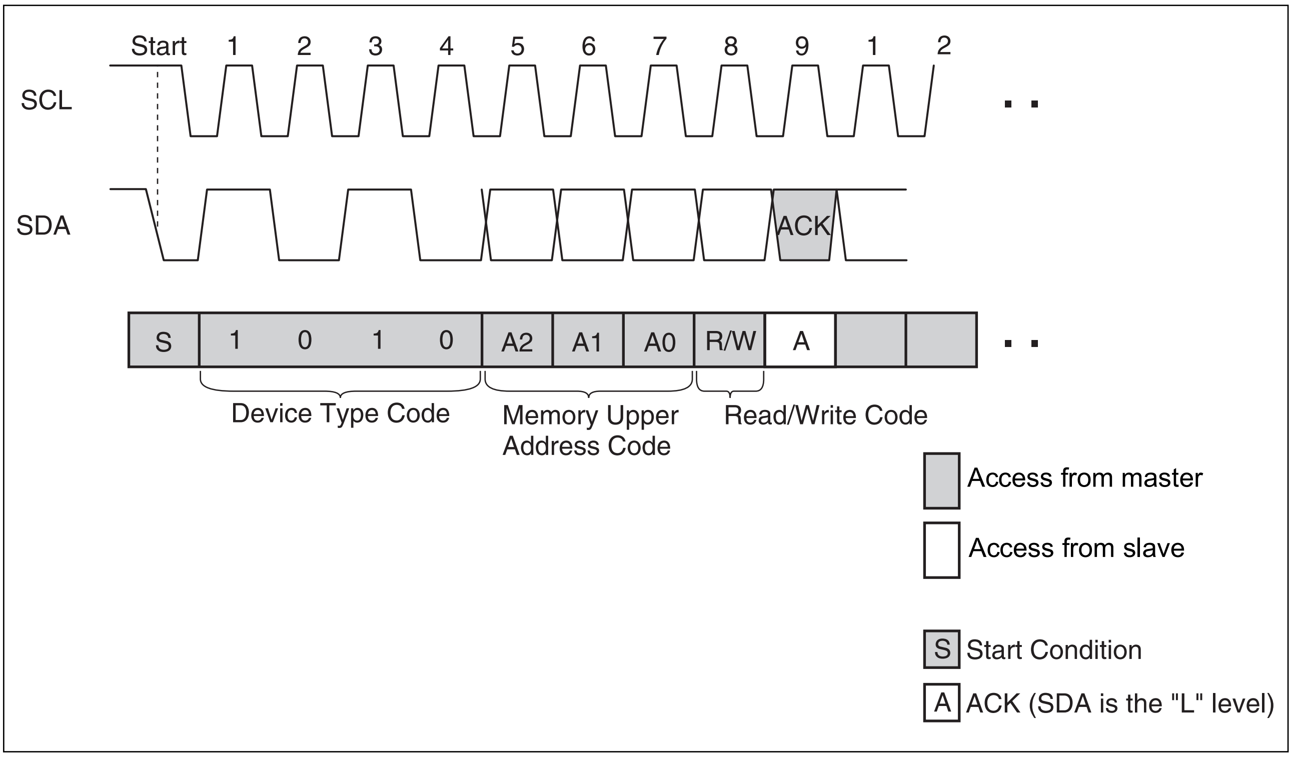
Following the device type code, the 3 bits of the memory upper address code are input.

The slave address selection is not performed by the external pin setting on this device. These 3 bits are not the setting bits for the slave address, but the upper 3-bit setting bits for the memory address.

- Read/Write Code (1 bit)

The 8th bit of the device address word is the R/W (Read/Write) code. When the R/W code is “0” input, a write operation is enabled, and the R/W code is “1” input, a read operation is enabled for the MB85RC16V. If the device code is not “1010”, the Read/Write operation is not performed and the standby state is chosen.

**• Device Address Word**



## ■ DATA STRUCTURE

The master inputs the device address word (8 bits) following the start condition, and then the slave outputs the Acknowledge “L” level on the 9th bit. After confirming the Acknowledge response, the sequential 8-bit memory lower address is input, to the byte write, page write and random read commands.

As for the current address read command, inputting the memory lower address is not performed, and the address buffer lower 8-bit is used as the memory lower address.

When inputting the memory lower address is finished, the slave outputs the Acknowledge “L” level on the 9th bit again.

Afterwards, the input and the output data continue in 8-bit units, and then the Acknowledge “L” level is output for every 8-bit data.

## ■ FeRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The MB85RC16V performs the high speed write operations, so any waiting time for an ACK* by the acknowledge polling does not occur.

*: In E$^2$PROM, the Acknowledge Polling is performed as a progress check whether rewriting is executed or not. It is normal to judge by the 9th bit of Acknowledge whether rewriting is performed or not after inputting the start condition and then the device address word (8 bits) during rewriting.

## ■ WRITE PROTECT (WP)

The entire memory array can be write protected by setting the WP pin to the “H” level. When the WP pin is set to the “L” level, the entire memory array will be rewritten. Reading is allowed regardless of the WP pin's “H” level or “L” level.

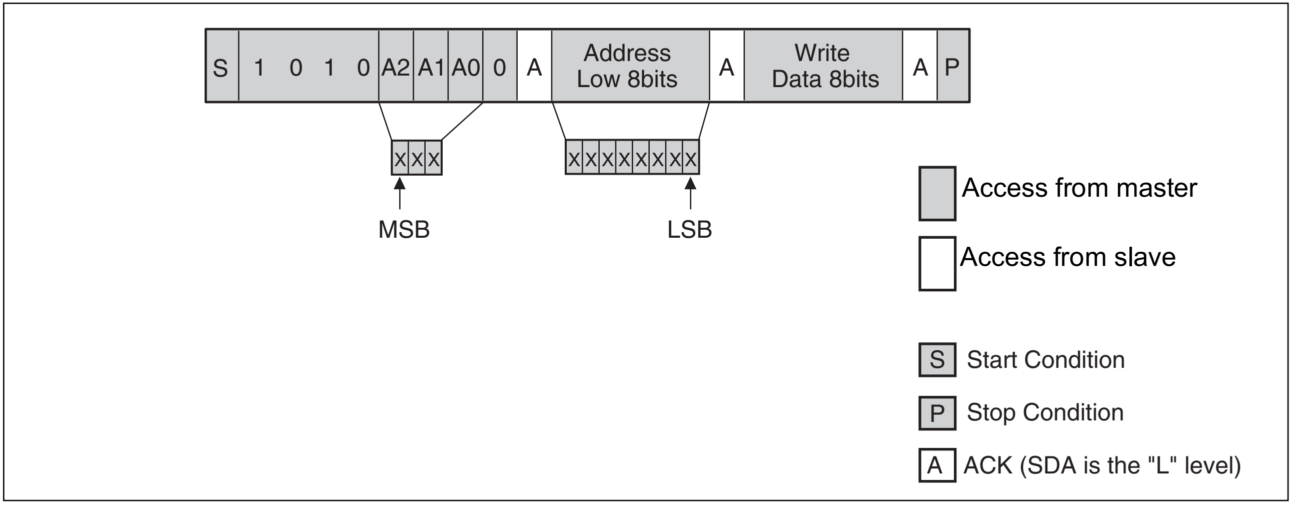
Do not change the WP signal level during the communication period from the start condition to the stop condition.

Note : The WP pin is pulled down internally to the VSS pin, therefore if the WP pin is open, the pin status is recognized as the “L” level (write enabled).

## ■ COMMAND

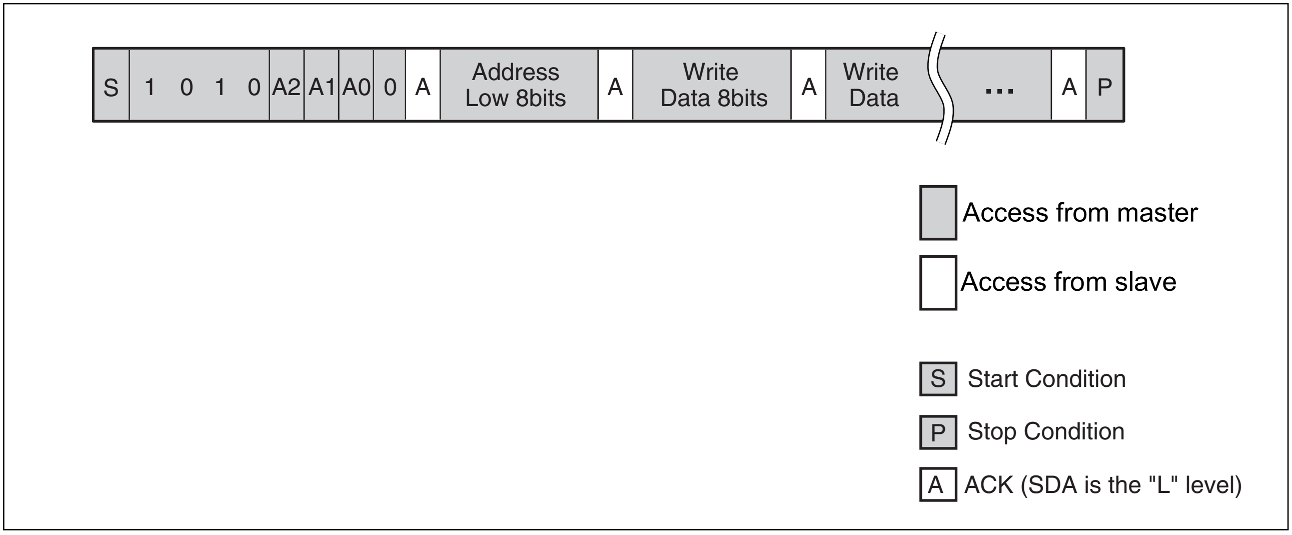
- Byte Write

If the device address word (R/W “0” input) is sent after the start condition, the slave responds with an ACK. After this ACK, write memory addresses and write data are sent in the same way, and the write ends by generating a stop condition at the end.


S
1 0 1 0
A2
A1
A0
0
A
Address Low 8bits
A
Write Data 8bits
A
P
xxx
xxxxxxxx
MSB
LSB
Access from master
Access from slave
S Start Condition
P Stop Condition
A ACK (SDA is the "L" level)

- Page Write

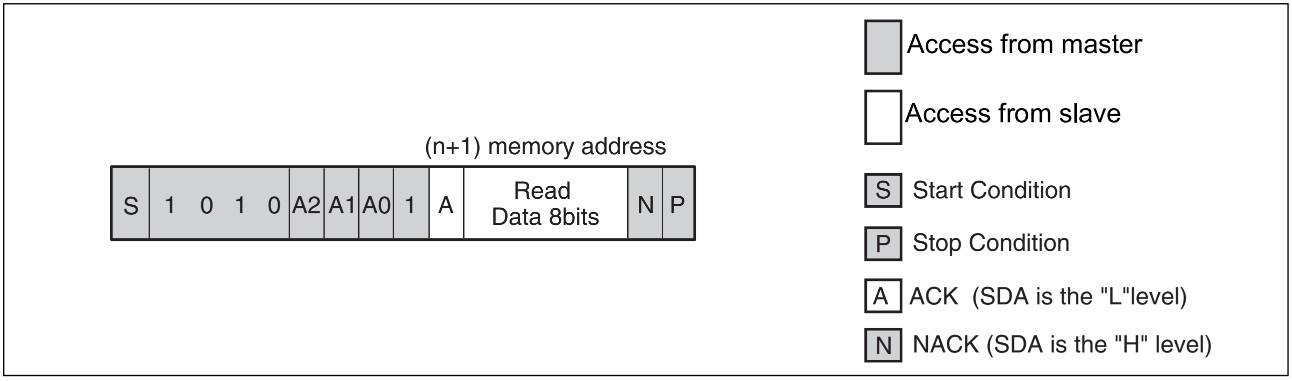
If additional 8 bits are continuously sent after the same command (except stop condition) as Byte Write, a page write is performed. The memory address rolls over to first memory address ($000_H$) at the end of the address. Therefore, if more than 2 Kbytes are sent, the data is overwritten in order starting from the start of the memory address that was written first.


S
1 0 1 0
A2
A1
A0
0
A
Address Low 8bits
A
Write Data 8bits
A
Write Data
...
A
P
Access from master
Access from slave
S Start Condition
P Stop Condition
A ACK (SDA is the "L" level)

- Current Address Read

If the last write or read operation finishes successfully up to the end of stop condition, the memory address that was accessed last remains in the memory address buffer (the length is 11 bits).

When sending this command without turning the power off, it is possible to read from the memory address n+1 which adds 1 to the total 11-bit memory address n, which consists of the memory upper address 3-bit from the device address word input and the lower 8-bit of the memory address buffer. If the memory address n is the last address, it is possible to read with rolling over to the head of the memory address ($000_H$). The current address (address that the memory address buffer indicates) is undefined immediately after turning the power on.

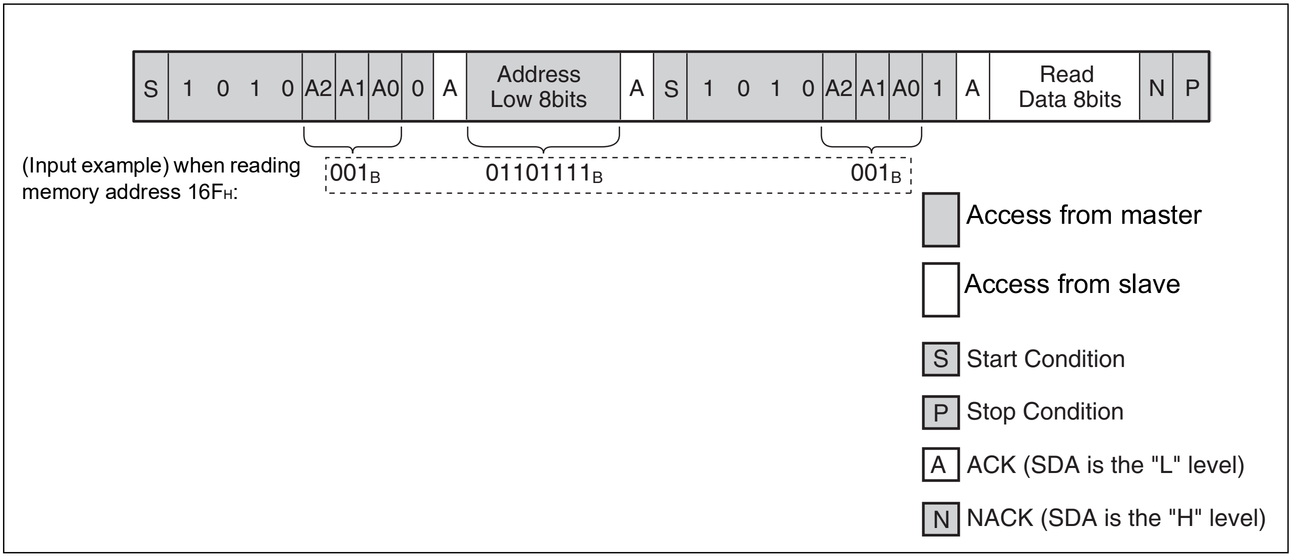

(n+1) memory address
S
1
0
1
0
A2
A1
A0
1
A
Read Data 8bits
N
P
Access from master
Access from slave
S Start Condition
P Stop Condition
A ACK (SDA is the "L"level)
N NACK (SDA is the "H" level)

- Random Read

The one byte of data from the memory address saved in the memory address buffer can be read out synchronously to SCL by specifying the address in the same way as for a write, and then issuing another start condition and sending the Device Address Word (R/W “1” input).

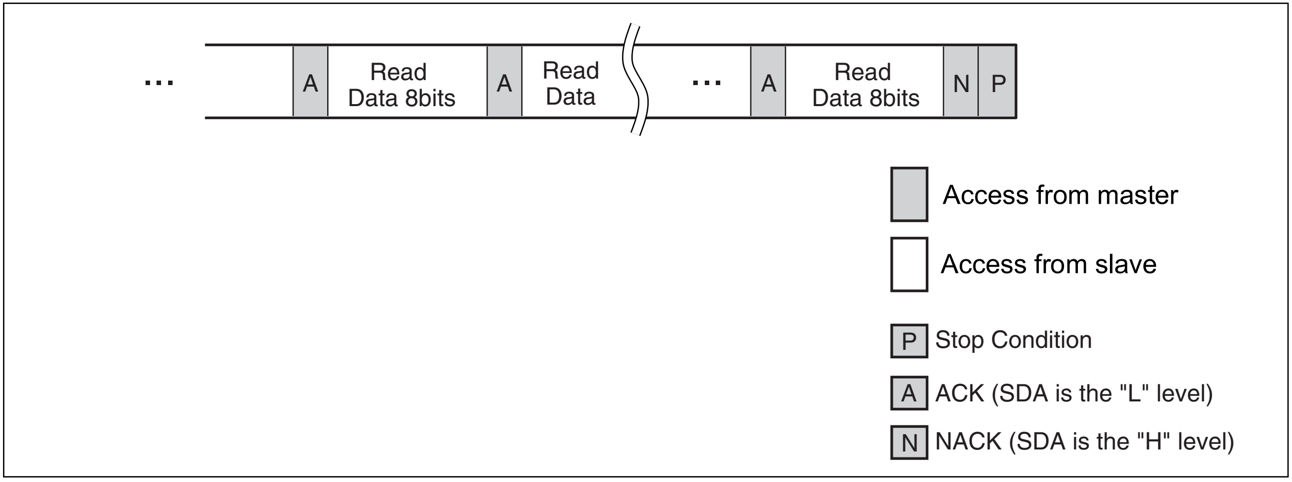
Setting values for the first and the second memory upper address codes should be the same (an example is shown in below).

The final NACK (SDA is the “H” level) is issued by the receiver that receives the data. In this case, this bit is issued by the master side.


S
1
0
1
0
A2
A1
A0
0
A
Address Low 8bits
A
S
1
0
1
0
A2
A1
A0
1
A
Read Data 8bits
N
P
(Input example) when reading memory address 16FH:
001B
01101111B
001B
Access from master
Access from slave
S Start Condition
P Stop Condition
A ACK (SDA is the "L" level)
N NACK (SDA is the "H" level)

- Sequential Read

Data can be received continuously following the Device address word (R/W “1” input) after specifying the address in the same way as for Random Read. If the read reaches the end of address, the read address automatically rolls over to the first memory address (000H) and keeps reading.

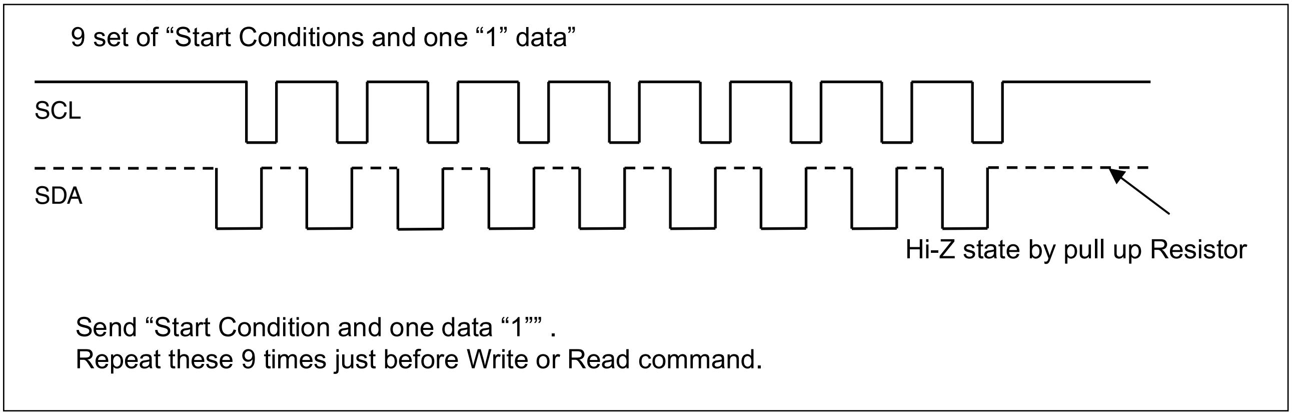

…
A
Read Data 8bits
A
Read Data
…
A
Read Data 8bits
N
P
Access from master
Access from slave
P Stop Condition
A ACK (SDA is the "L" level)
N NACK (SDA is the "H" level)

## ■ SOFTWARE RESET SEQUENCE OR COMMAND RETRY

In case the malfunction has occurred after power on, the master side stopped the I²C communication during processing, or unexpected malfunction has occurred, execute the following (1) software recovery sequence just before each command, or (2) retry command just after failure of each command.

### (1) Software Reset Sequence

Since the slave side may be outputting “L” level, do not force to drive “H” level, when the master side drives the SDA port. This is for preventing a bus conflict. The additional hardware is not necessary for this software reset sequence.


9 set of “Start Conditions and one “1” data”
SCL
SDA
Hi-Z state by pull up Resistor

Send “Start Condition and one data “1”” .
Repeat these 9 times just before Write or Read command.

### (2) Command Retry

Command retry is useful to recover from failure response during I²C communication.

## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating |  | Unit |
|---|---|---|---|---|
|  |  | Min | Max |  |
| Power supply voltage* | $V_{DD}$ | – 0.5 | + 6.0 | V |
| Input voltage* | $V_{IN}$ | – 0.5 | $V_{DD}$ + 0.5 ( ≤ 6.0) | V |
| Output voltage* | $V_{OUT}$ | – 0.5 | $V_{DD}$ + 0.5 ( ≤ 6.0) | V |
| Operation ambient temperature | $T_A$ | – 40 | + 85 | °C |
| Storage temperature | $T_{STG}$ | – 55 | + 125 | °C |

*: These parameters are based on the condition that Vss is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value |  |  | Unit |
|---|---|---|---|---|---|
|  |  | Min | Typ | Max |  |
| Power supply voltage[*1] | $V_{DD}$ | 3.0 | — | 5.5 | V |
| Operation ambient temperature[*2] | $T_A$ | – 40 | — | + 85 | °C |

*1: These parameters are based on the condition that Vss is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Input leakage current*[1] | $\|I_{LI}\|$ | $V_{IN}$ = 0 V to $V_{DD}$ | — | — | 1 | μA |
| Output leakage current*[2] | $\|I_{LO}\|$ | $V_{OUT}$ = 0 V to $V_{DD}$ | — | — | 1 | μA |
| Operating power supply current | $I_{DD}$ | SCL = 400 kHz | — | 40 | 80 | μA |
| | | SCL = 1000 kHz | — | 90 | 130 | μA |
| Standby current | $I_{SB}$ | SCL, SDA = $V_{DD}$<br>WP = 0 V or $V_{DD}$ or OPEN<br>$T_A$ = + 25 °C in stop condition | — | 5 | 10 | μA |
| “H” level input voltage | $V_{IH}$ | $V_{DD}$ = 3.0 V to 5.5 V | $V_{DD}$ × 0.8 | — | 5.5 | V |
| “L” level input voltage | $V_{IL}$ | $V_{DD}$ = 3.0 V to 5.5 V | $V_{SS}$ | — | $V_{DD}$ × 0.2 | V |
| “L” level output voltage | $V_{OL}$ | $I_{OL}$ = 3 mA | — | — | 0.4 | V |
| Input resistance for WP pin | $R_{IN}$ | $V_{IN}$ = $V_{IL}$ (Max) | 50 | — | — | kΩ |
| | | $V_{IN}$ = $V_{IH}$ (Min) | 1 | — | — | MΩ |

*1: Applicable pin: SCL,SDA

*2: Applicable pin: SDA

## 2. AC Characteristics

| Parameter | Symbol | Value | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | STANDARD MODE | | FAST MODE | | FAST MODE PLUS | | |
| | | Min | Max | Min | Max | Min | Max | |
| SCL clock frequency | FSCL | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| Clock high time | $T_{HIGH}$ | 4000 | — | 600 | — | 400 | — | ns |
| Clock low time | $T_{LOW}$ | 4700 | — | 1300 | — | 600 | — | ns |
| SCL/SDA rising time | $T_r$ | — | 1000 | — | 300 | — | 300 | ns |
| SCL/SDA falling time | $T_f$ | — | 300 | — | 300 | — | 100 | ns |
| Start condition hold | $T_{HD:STA}$ | 4000 | — | 600 | — | 250 | — | ns |
| Start condition setup | $T_{SU:STA}$ | 4700 | — | 600 | — | 250 | — | ns |
| SDA input hold | $T_{HD:DAT}$ | 20 | — | 20 | — | 20 | — | ns |
| SDA input setup | $T_{SU:DAT}$ | 250 | — | 100 | — | 100 | — | ns |
| SDA output hold | $T_{DH:DAT}$ | 0 | — | 0 | — | 0 | — | ns |
| Stop condition setup | $T_{SU:STO}$ | 4000 | — | 600 | — | 250 | — | ns |
| SDA output access after SCL falling | $T_{AA}$ | — | 3000 | — | 900 | — | 550 | ns |
| Pre-charge time | $T_{BUF}$ | 4700 | — | 1300 | — | 500 | — | ns |
| Noise suppression time (SCL and SDA) | $T_{SP}$ | — | 50 | — | 50 | — | 50 | ns |

AC characteristics were measured under the following measurement conditions.

Power supply voltage : STANDARD MODE and FAST MODE 3.0 V to 5.5 V
: FAST MODE PLUS 4.5 V to 5.5 V

Operation ambient temperature: – 40 °C to + 85 °C

Input voltage amplitude: $V_{DD} \times 0.2$ to $V_{DD} \times 0.8$

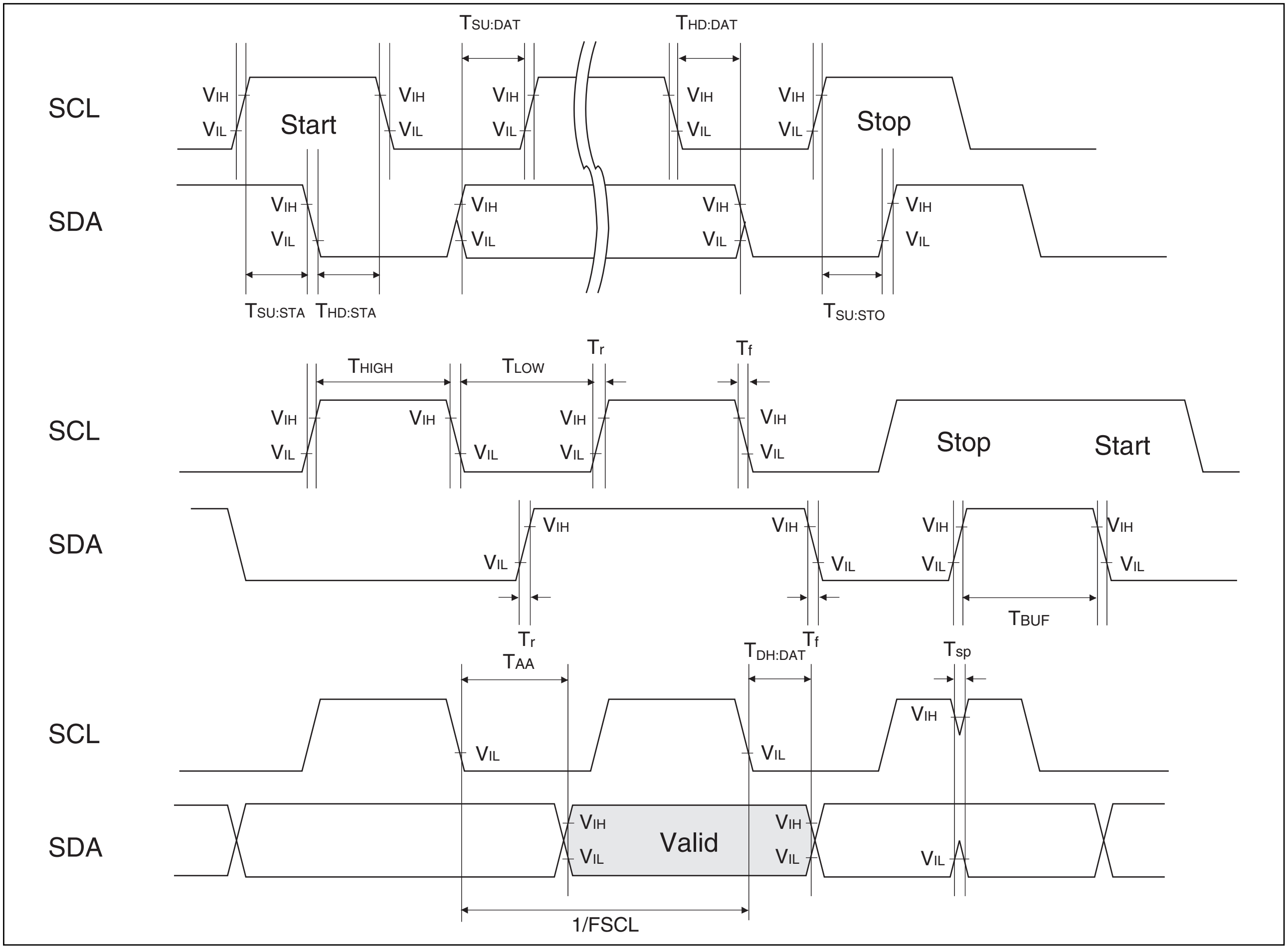
Input rising time : 5 ns

Input falling time : 5 ns

Input judge level : $V_{DD}/2$

Output judge level : $V_{DD}/2$

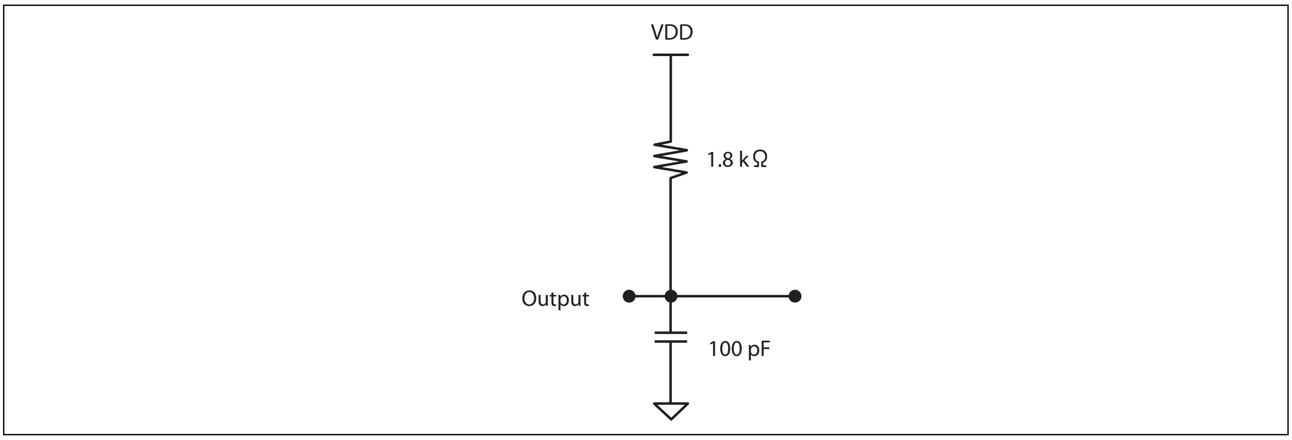
## 3. AC Timing Definitions


SCL
SDA
Start
Stop
VIH
VIL
TSU:DAT
THD:DAT
TSU:STA
THD:STA
TSU:STO
THIGH
TLOW
Tr
Tf
TBUF
TAA
TDH:DAT
Tsp
Valid
1/FSCL

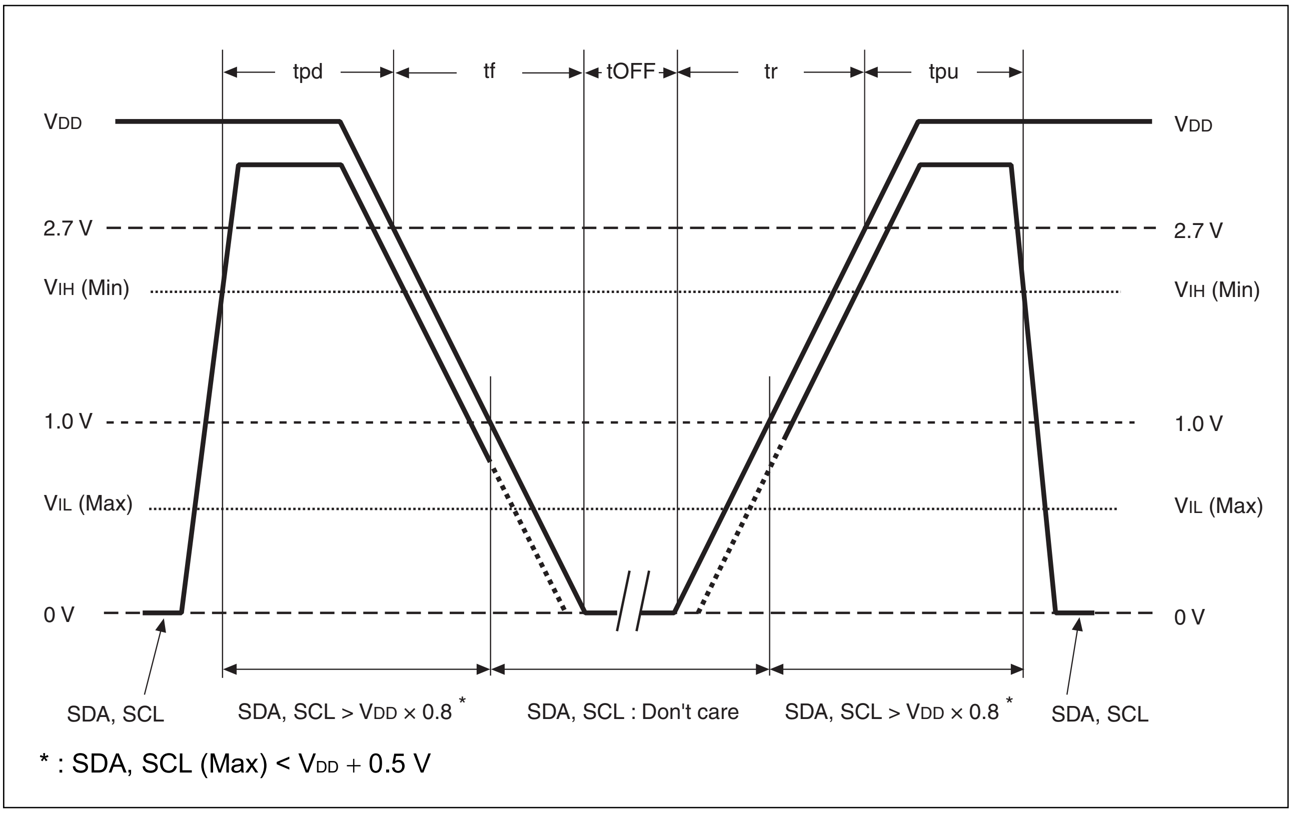
## 4. Pin capacitance

| Parameter | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| I/O capacitance | $C_{I/O}$ | $V_{DD} = V_{IN} = V_{OUT} = 0V$,<br>f = 1 MHz, $T_A = +25$ °C | — | — | 15 | pF |
| Input capacitance | $C_{IN}$ | | — | — | 15 | pF |

## 5. AC Test Load Circuit


VDD
1.8 kΩ
Output
100 pF

## ■ POWER ON/OFF SEQUENCE



| Parameter | Symbol | Value |  | Unit | Condition |
|---|---|---|---|---|---|
|  |  | Min | Max |  |  |
| SDA, SCL level hold time during power down | tpd | 85 | — | ns | — |
| SDA, SCL level hold time during power up | tpu | 85 | — | ns | $V_{DD}$ = 5.0V ± 0.5V Operation |
|  |  | 0.5 | — | ms | $V_{DD}$ = 3.3V ± 0.3V Operation |
| Power supply rising time | tr | 0.5 | 50 | ms | $V_{DD}$ = 5.0V ± 0.5V Operation |
|  |  | 0.005 | 50 |  | $V_{DD}$ = 3.3V ± 0.3V Operation |
| Power supply falling time | tf | 0.01 | 50 | ms | — |
| Power off time | tOFF | 50 | — | ms | — |

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

## ■ FeRAM CHARACTERISTICS

| Item | Min | Max | Unit | Parameter |
|---|---|---|---|---|
| Read/Write Endurance*1 | $10^{12}$ | — | Times/byte | Operation Ambient Temperature $T_A$ = + 85 °C |
| Data Retention*2 | 10 | — | Years | Operation Ambient Temperature $T_A$ = + 85 °C |
|  | 95 | — |  | Operation Ambient Temperature $T_A$ = + 55 °C |
|  | ≥ 200 | — |  | Operation Ambient Temperature $T_A$ = + 35 °C |

*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

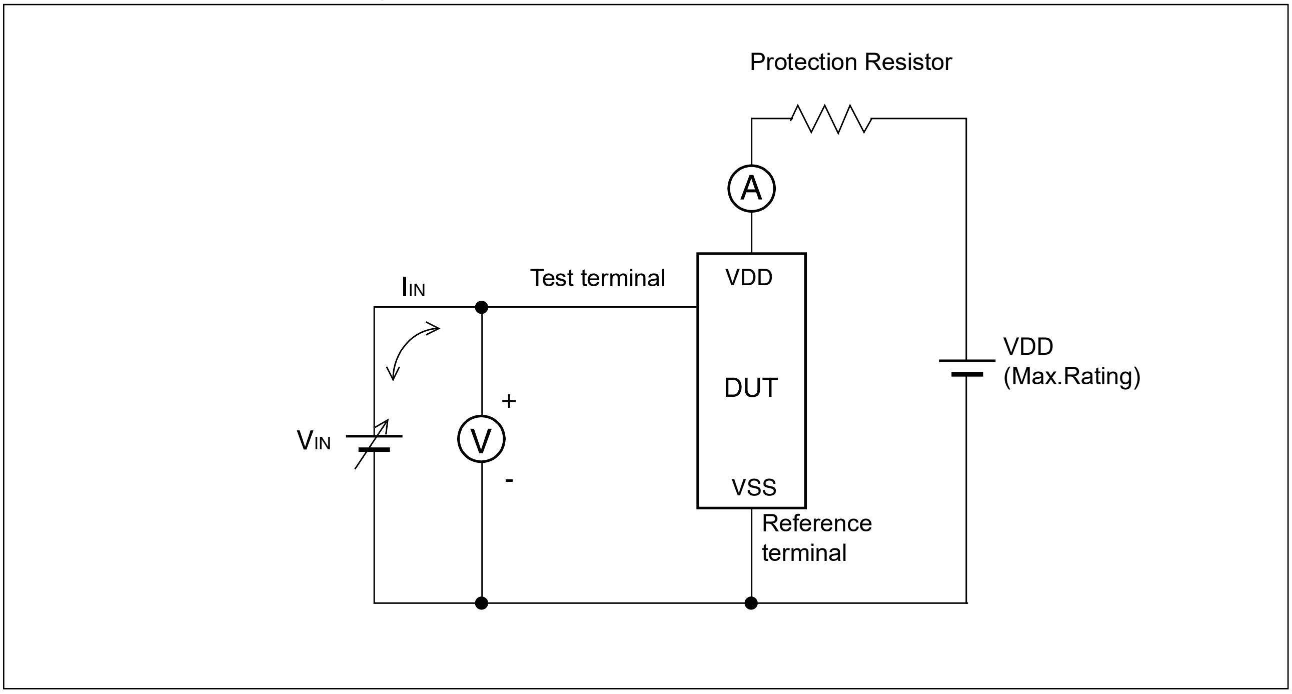
## ■ NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

## ■ ESD AND LATCH-UP

| Test | DUT | Value |
|---|---|---|
| ESD HBM (Human Body Model)<br>JESD22-A114 compliant | MB85RC16VPNF-G-JNN1E1<br>MB85RC16VPNF-G-JNN1ERE1<br>MB85RC16VPNF-G-AWE2<br>MB85RC16VPNF-G-AWERE2 | ≥ \|2000 V\| |
| ESD CDM (Charged Device Model)<br>JESD22-C101 compliant | | ≥ \|1000 V\| |
| Latch-Up (Current Method)<br>Proprietary method | | ≥ \|300 mA\| |

- Current method of Latch-Up Resistance Test


Protection Resistor
A
$I_{IN}$
Test terminal
VDD
DUT
VSS
VDD
(Max.Rating)
+
V
-
$V_{IN}$
Reference
terminal

Note : The voltage $V_{IN}$ is increased gradually and the current $I_{IN}$ of 300 mA at maximum shall flow.
Confirm the latch up does not occur under $I_{IN}$ = ± 300 mA.
In case the specific requirement is specified for I/O and $I_{IN}$ cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

## ■ REFLOW CONDITIONS AND FLOOR LIFE

[ JEDEC MSL ] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

## ■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

## ■ ORDERING INFORMATION

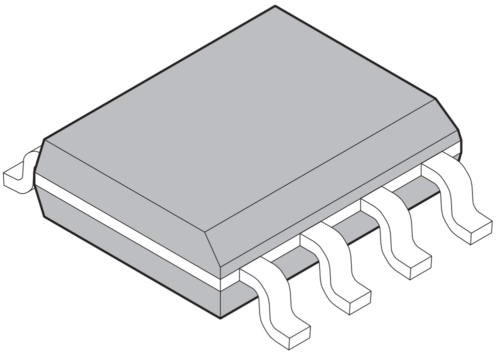
| Part number | Package | Shipping form | Minimum shipping quantity |
|---|---|---|---|
| MB85RC16VPNF-G-JNN1E1 | 8-pin, plastic SOP (150mil) | Tube | —[*1] |
| MB85RC16VPNF-G-JNN1ERE1 | 8-pin, plastic SOP (150mil) | Embossed Carrier tape | 1500 |
| MB85RC16VPNF-G-AWE2 | 8-pin, plastic SOP (150mil) | Tube | —[*1] |
| MB85RC16VPNF-G-AWERE2 | 8-pin, plastic SOP (150mil) | Embossed Carrier tape | 1500 |

*1: Please contact our sales office about minimum shipping quantity.

## ■ PACKAGE DIMENSION

### ■ (1)MB85RC16VPNF-G-JNN1E1/MB85RC16VPNF-G-JNN1ERE1

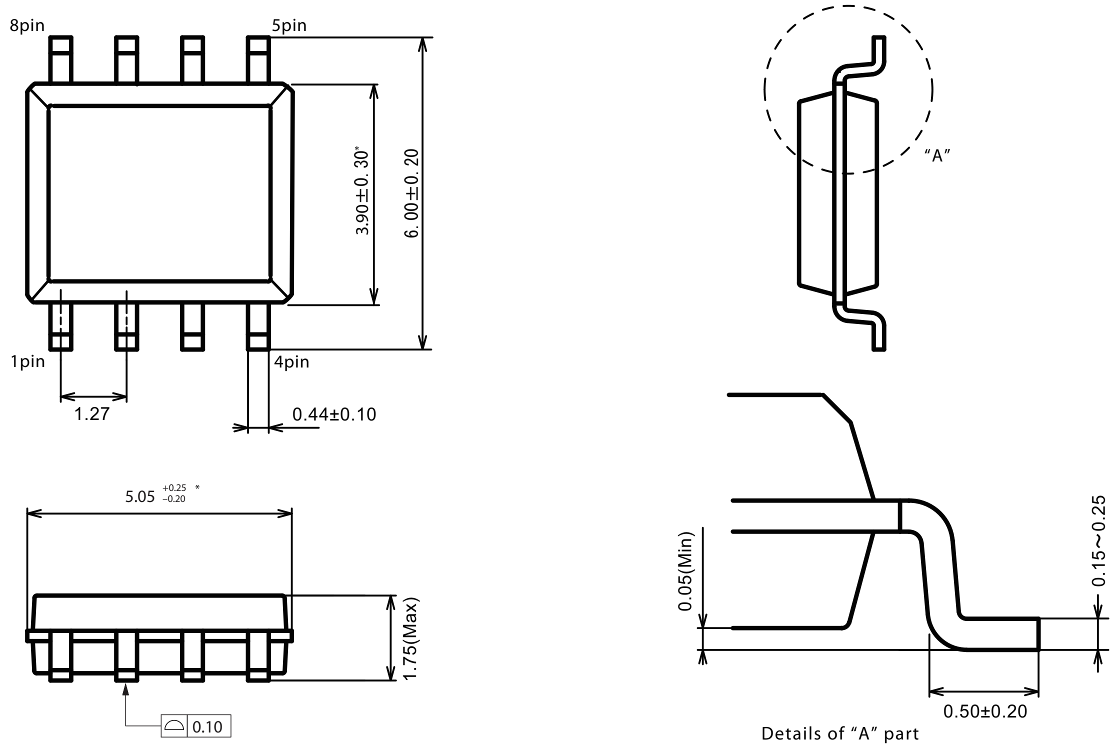
8-pin plastic SOP



| | |
|---|---|
| Lead pitch | 1.27 mm |
| Package width × package length | 3.90 mm × 5.05 mm |
| Lead shape | Gullwing |
| Sealing method | Plastic mold |
| Mounting heigth | 1.75 mm MAX |
| | |
| | |

8-pin plastic SOP

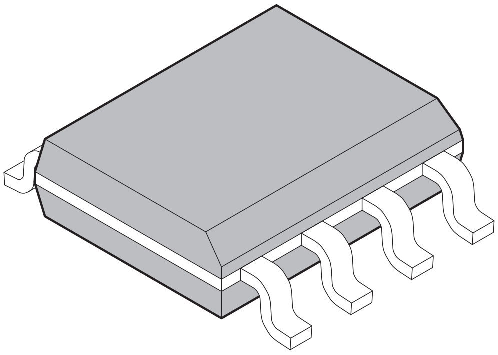
Note *: These dimensions do not include resin protrution.
Pins width and pins thickness include plating thickness.
Pins width not do ninclude tie bar cutting remaindar.


8pin
5pin
1pin
4pin
3.90±0. 30*
6. 00±0. 20
1.27
0.44±0.10
5.05 +0.25 −0.20 *
1.75(Max)
0.10
"A"
0.05(Min)
0.15~0.25
0.50±0.20
Details of "A" part

Dimenssions in mm

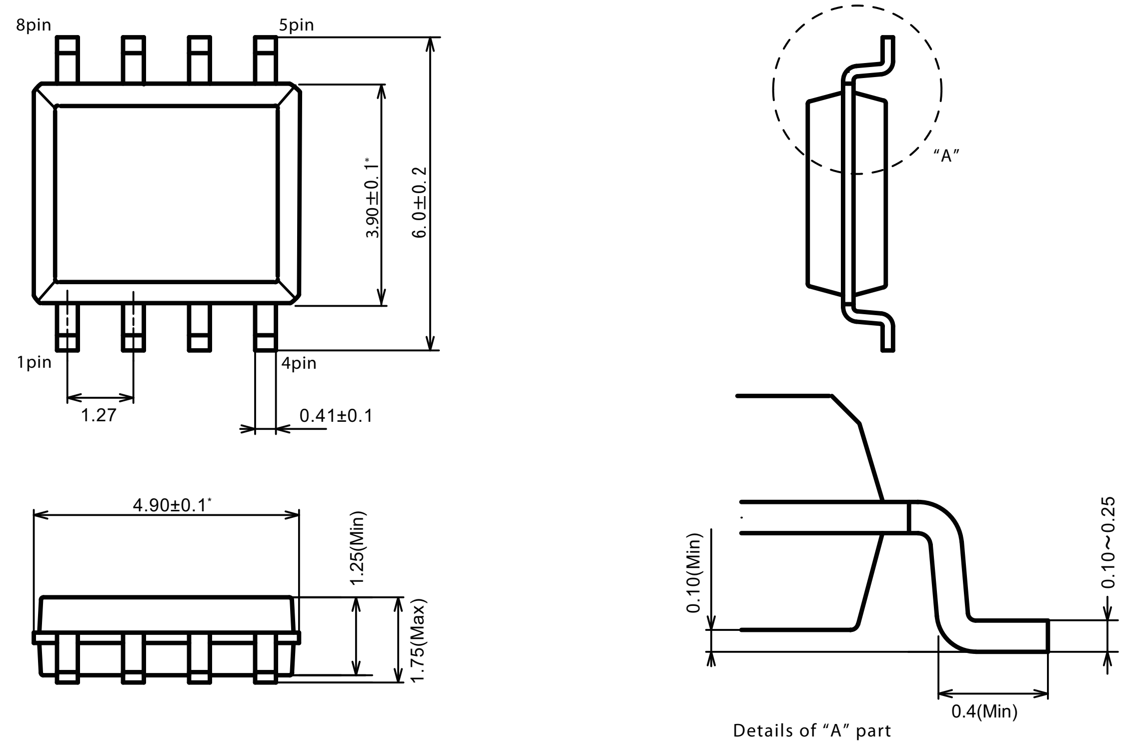
*(continued)*

## ■ (2)MB85RC16VPNF-G-AWE2/MB85RC16VPNF-G-AWERE2

| | | |
|---|---|---|
| 8-pin plastic SOP<br> | Lead pitch | 1.27mm |
| | Package width × package length | 3.90mm × 4.90mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting heigth | 1.75mm MAX |
| | | |
| | | |

8-pin plastic SOP

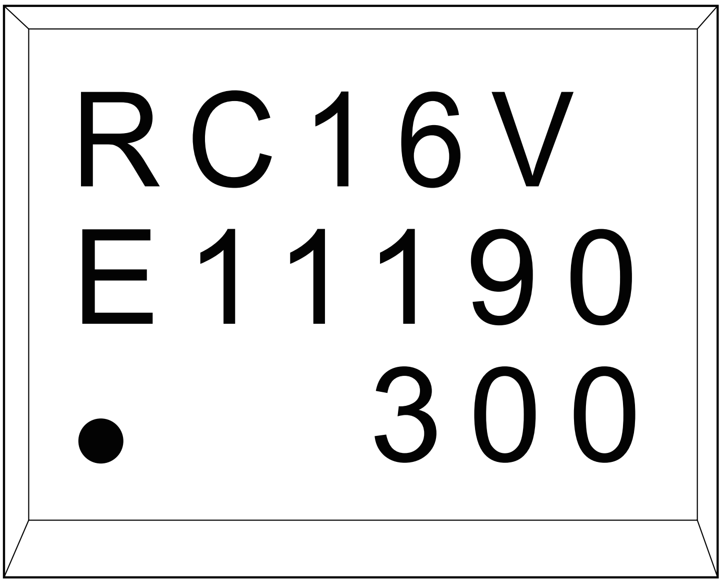
Note *: These dimensions do not include resin protrution.
Pins width not do ninclude tie bar cutting remaindar.


8pin
5pin
3.90±0.1*
6.0±0.2
1pin
4pin
1.27
0.41±0.1
4.90±0.1*
1.25(Min)
1.75(Max)
"A"
0.10(Min)
0.10~0.25
0.4(Min)
Details of "A" part

Dimenssions in mm

## ■ MARKING (example)

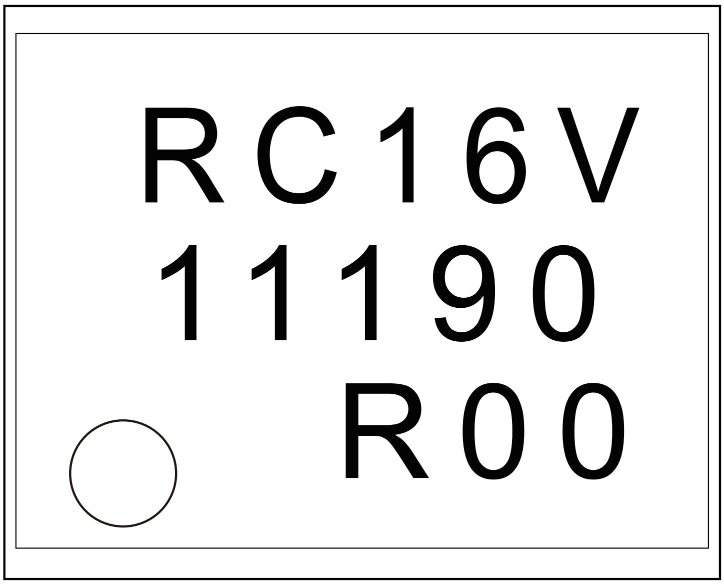
[MB85RC16VPNF-G-JNN1E1]
[MB85RC16VPNF-G-JNN1ERE1]



[8-pin plastic SOP]

RC16V : Product name
E11900 : E1(Lead free code) + 1190(Year and Week code)
300: Trace code

[MB85RC16VPNF-G-AWE2
[MB85RC16VPNF-G-AWERE2]



[8-pin plastic SOP]

RC16V : Product name
11900 : 1(CS code) + 1190(Year and Week code)
R00: Trace code

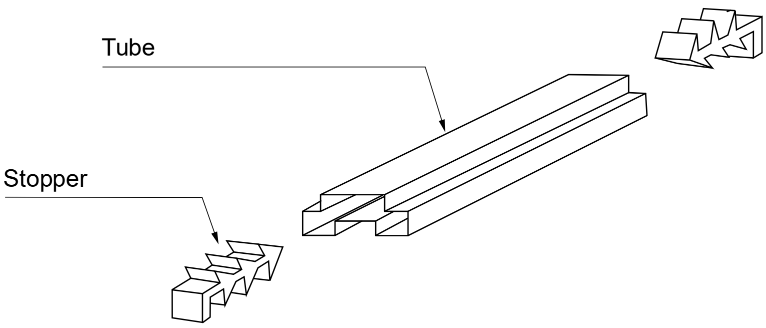
## ■ PACKING INFORMATION

### (1)MB85RC16VPNF-G-JNN1E1/MB85RC16VPNF-G-JNN1ERE1

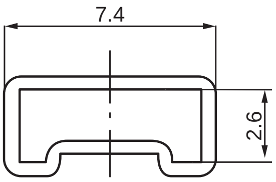
### 1. Tube (MB85RC16VPNF-G-JNN1E1)

### 1.1 Tube Dimensions

- Tube/stopper shape (example)

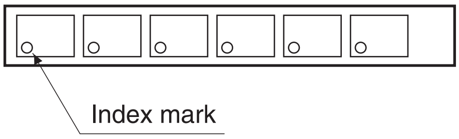


- **Tube cross-sections and Maximum quantity**

| Package form | Maximum quantity | | |
|---|---|---|---|
| | ICs/tube(520mm) | ICs/inner box | ICs/outer box |
|  | 95 | 7,600 | 30,400 |
| | No heat resistance.<br>Package should not be baked by using tube. | | |

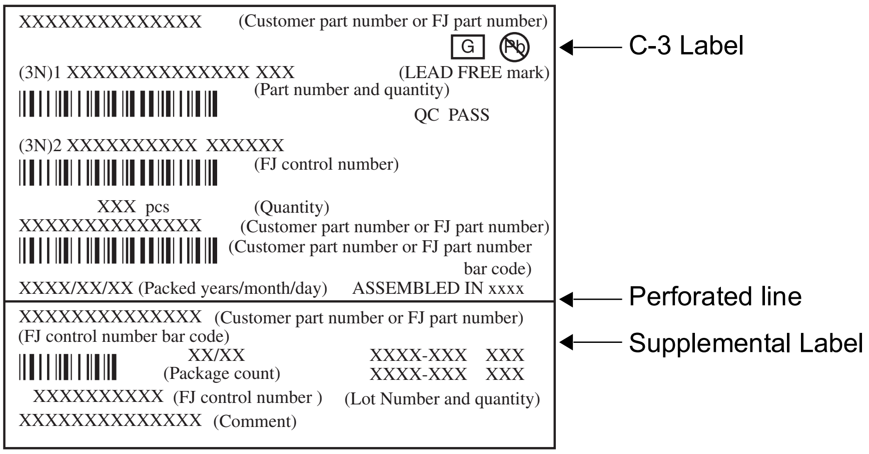
(Dimensions in mm)

- **Direction of index of tube**



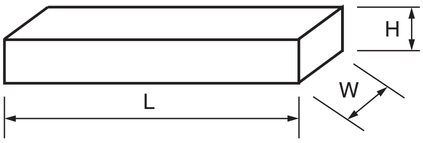
### 1.2 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]


XXXXXXXXXXXXXX (Customer part number or FJ part number)
G
Pb
C-3 Label
(3N)1 XXXXXXXXXXXXXX XXX
(LEAD FREE mark)
(Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX
(FJ control number)
XXX pcs
(Quantity)
XXXXXXXXXXXXXX (Customer part number or FJ part number)
(Customer part number or FJ part number bar code)
XXXX/XX/XX (Packed years/month/day)
ASSEMBLED IN xxxx
Perforated line
XXXXXXXXXXXXXX (Customer part number or FJ part number)
Supplemental Label
(FJ control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (FJ control number )
(Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)

### 1.3 Dimensions for Containers

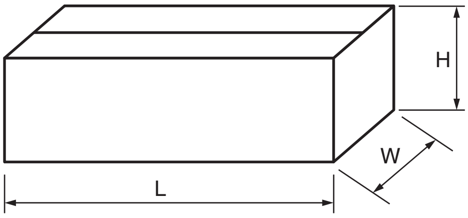
#### (1) Dimensions for inner box



| L | W | H |
|---|---|---|
| 540 | 125 | 75 |

(Dimensions in mm)

#### (2) Dimensions for outer box



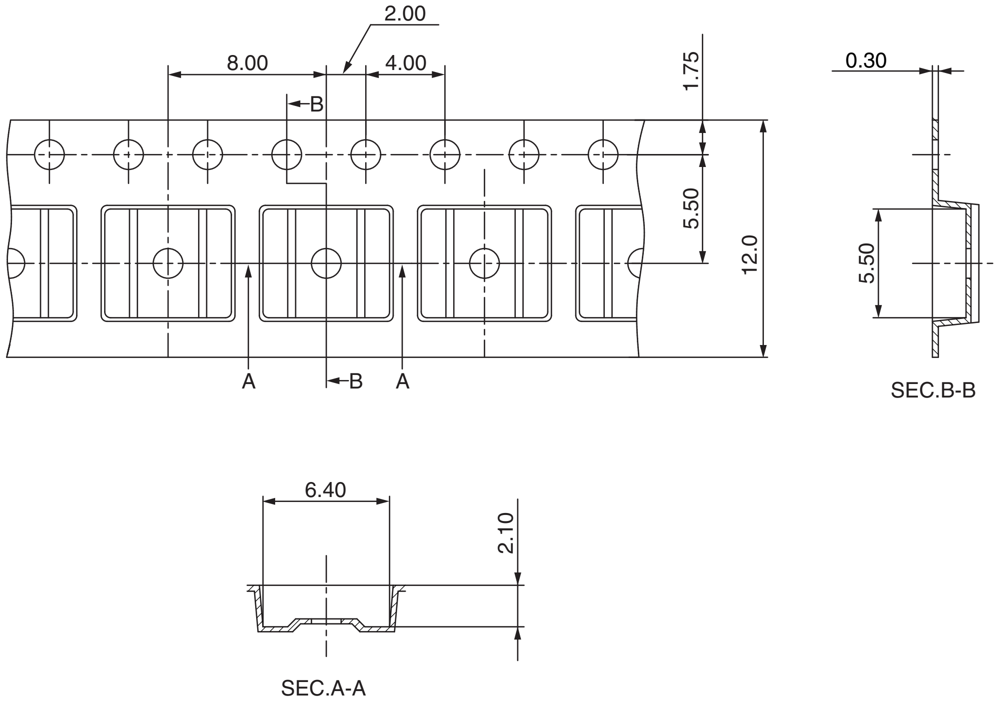
| L | W | H |
|---|---|---|
| 565 | 270 | 180 |

(Dimensions in mm)

## 2. Emboss Tape (MB85RC16VPNF-G-JNN1ERE1)

### 2.1 Tape Dimensions

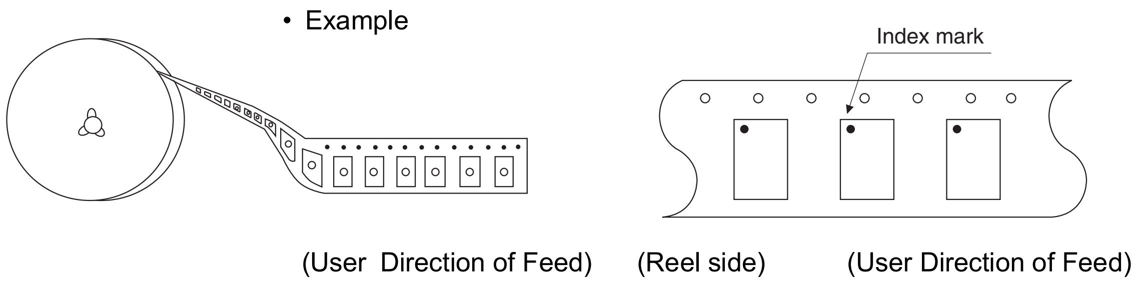
| Maximum storage capacity | | |
|---|---|---|
| ICs/reel(ϕ=330mm) | ICs/inner box | ICs/outer box |
| 1,500 | 1,500<br>(1 pack/inner box) | 10,500<br>(7 inner boxes/outer box: Max.) |


2.00
8.00
4.00
1.75
0.30
B
5.50
12.0
5.50
A
B
A
SEC.B-B
6.40
2.10
SEC.A-A

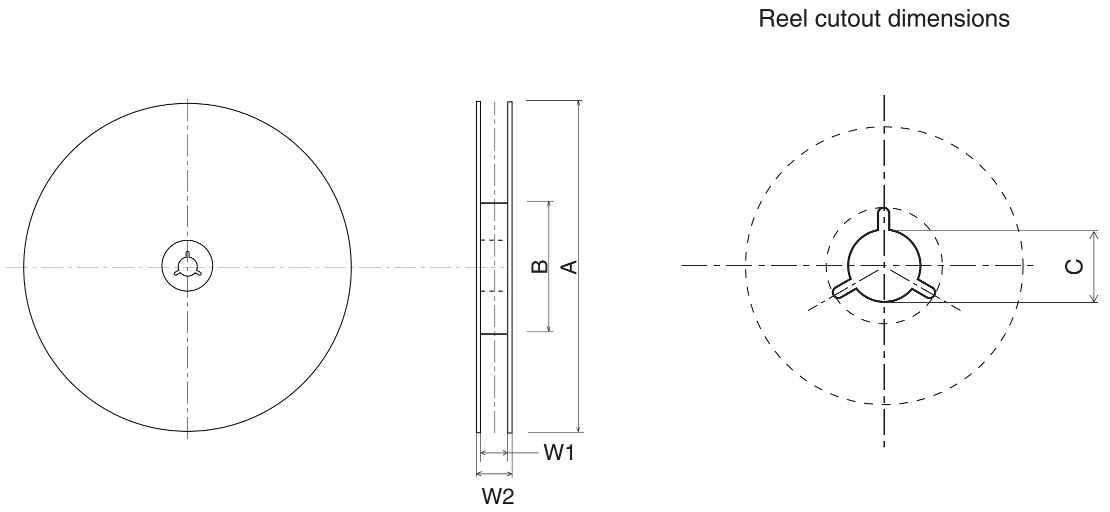
(Dimensions in mm)

Heat proof temperature : No heat resistance.
Package should not be baked by using tape and reel.

## 2.2 IC orientation


• Example
Index mark
(User Direction of Feed)
(Reel side)
(User Direction of Feed)

## 2.3 Reel dimensions

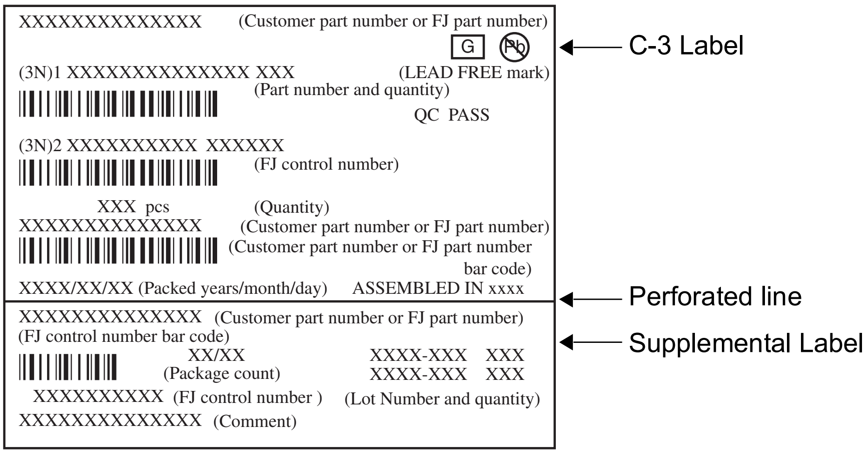

Reel cutout dimensions
A
B
C
W1
W2

Dimensions in mm

| A | B | C | W1 | W2 |
|---|---|---|---|---|
| 330 | 100 | 13 | 12.4 | 18.4 |

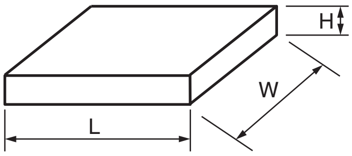
## 2.4 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]


XXXXXXXXXXXXXX (Customer part number or FJ part number)
G
Pb
(3N)1 XXXXXXXXXXXXXX XXX
(LEAD FREE mark)
(Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX
(FJ control number)
XXX pcs
(Quantity)
XXXXXXXXXXXXXX
(Customer part number or FJ part number)
(Customer part number or FJ part number bar code)
XXXX/XX/XX (Packed years/month/day)
ASSEMBLED IN xxxx
XXXXXXXXXXXXXX (Customer part number or FJ part number)
(FJ control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (FJ control number )
(Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)
C-3 Label
Perforated line
Supplemental Label

### 2.5 Dimensions for Containers

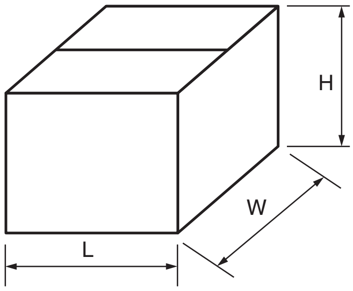
**(1) Dimensions for inner box**



| L | W | H |
|---|---|---|
| 365 | 345 | 40 |

(Dimensions in mm)

**(2) Dimensions for outer box**



| L | W | H |
|---|---|---|
| 415 | 400 | 315 |

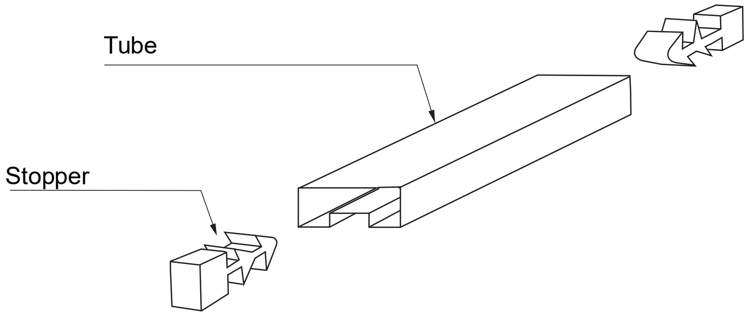
(Dimensions in mm)

(2)MB85RC16VPNF-G-AWE2/MB85RC16VPNF-G-AWERE2

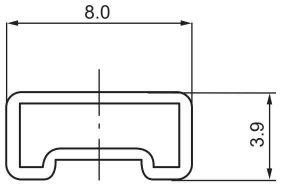
## 1. Tube (MB85RC16VPNF-G-AWE2)

### 1.1 Tube Dimensions

- Tube/stopper shape (example)

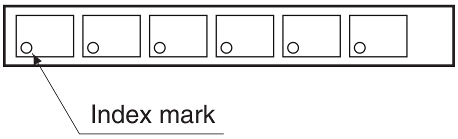


- **Tube cross-sections and Maximum quantity**

| Package form | Maximum quantity | | |
|---|---|---|---|
| | ICs/tube(509mm) | ICs/inner box | ICs/outer box |
|  | 85 | 4,250 | 25,500 |
| | No heat resistance.<br>Package should not be baked by using tube. | | |

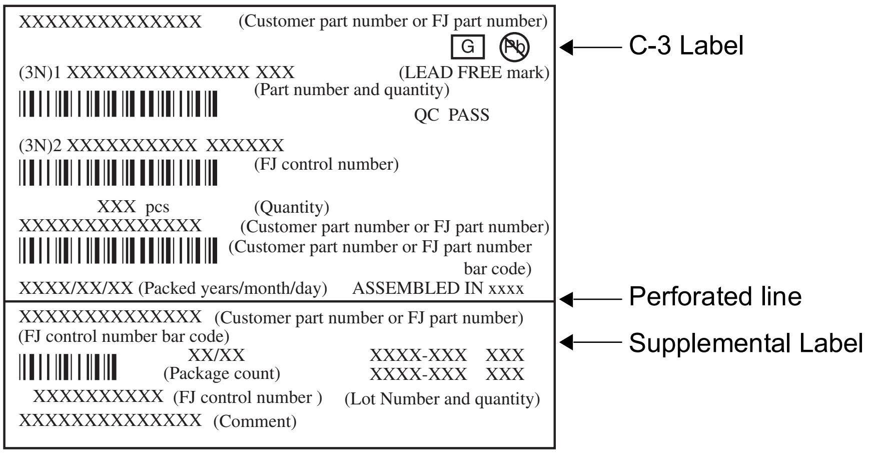
(Dimensions in mm)

- **Direction of index of tube**



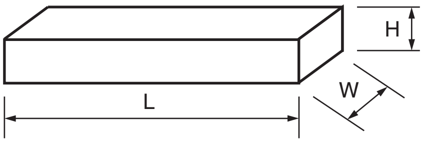
## 1.2 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]


XXXXXXXXXXXXXX (Customer part number or FJ part number)
G
Pb
(3N)1 XXXXXXXXXXXXXX XXX
(LEAD FREE mark)
(Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX
(FJ control number)
XXX pcs
(Quantity)
XXXXXXXXXXXXXX (Customer part number or FJ part number)
(Customer part number or FJ part number bar code)
XXXX/XX/XX (Packed years/month/day)
ASSEMBLED IN xxxx
XXXXXXXXXXXXXX (Customer part number or FJ part number)
(FJ control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (FJ control number )
(Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)
C-3 Label
Perforated line
Supplemental Label

### 1.3 Dimensions for Containers

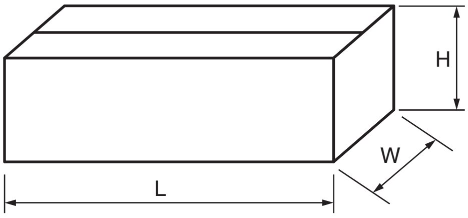
#### (1) Dimensions for inner box



| L | W | H |
|---|---|---|
| 549 | 125 | 81 |

(Dimensions in mm)

#### (2) Dimensions for outer box



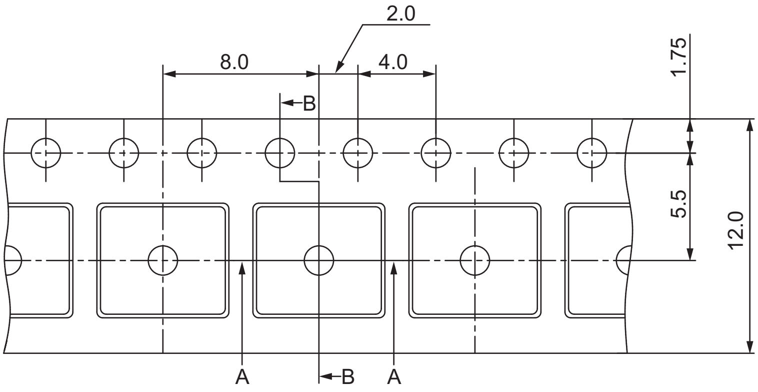
| L | W | H |
|---|---|---|
| 567 | 272 | 269 |

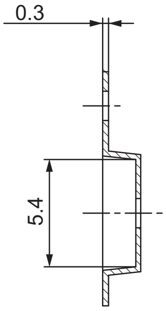
(Dimensions in mm)

## 2. Emboss Tape (MB85RC16VPNF-G-AWERE2)

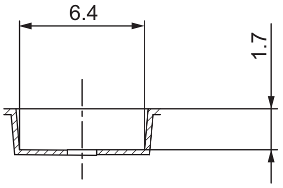
### 2.1 Tape Dimensions

| Maximum storage capacity | | |
|---|---|---|
| ICs/reel(ϕ=330mm) | ICs/inner box | ICs/outer box |
| 1,500 | 1,500<br>(1 pack/inner box) | 9,000<br>(6 inner boxes/outer box:Max.) |





SEC.B-B

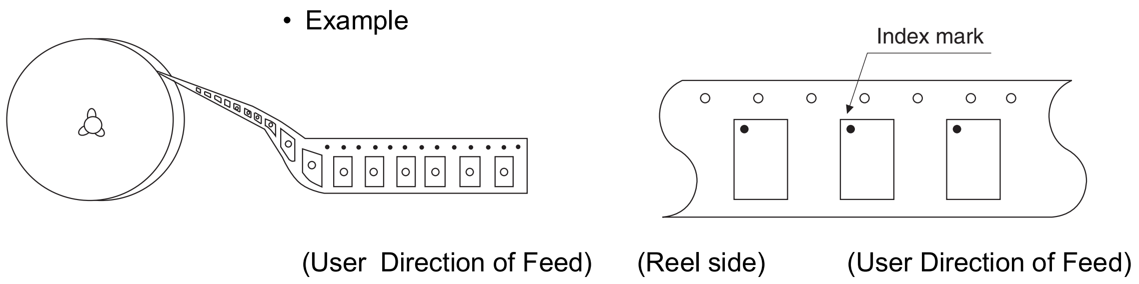


SEC.A-A

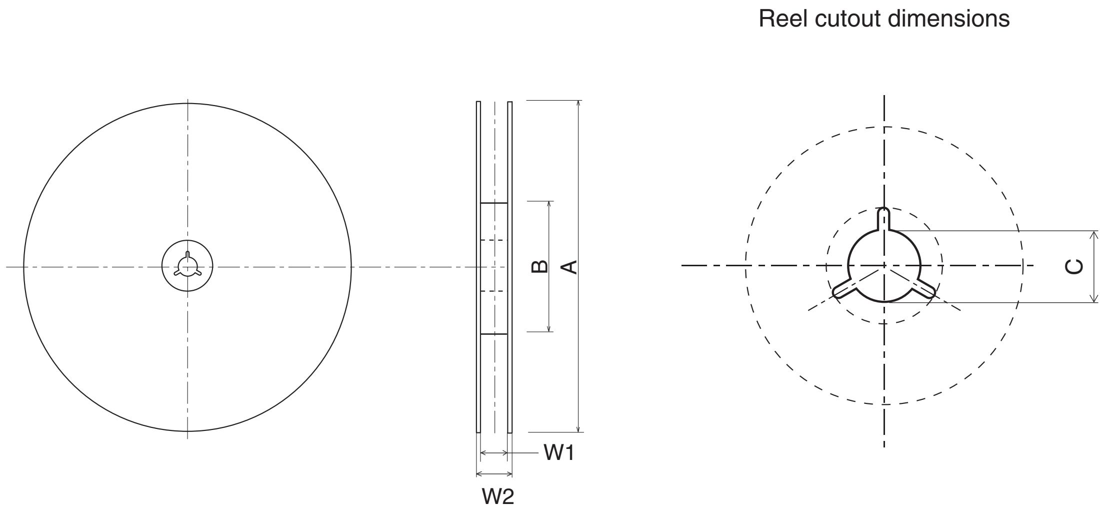
(Dimensions in mm)

Heat proof temperature : No heat resistance.
Package should not be baked by using tape and reel.

## 2.2 IC orientation


• Example
Index mark
(User Direction of Feed)
(Reel side)
(User Direction of Feed)

## 2.3 Reel dimensions

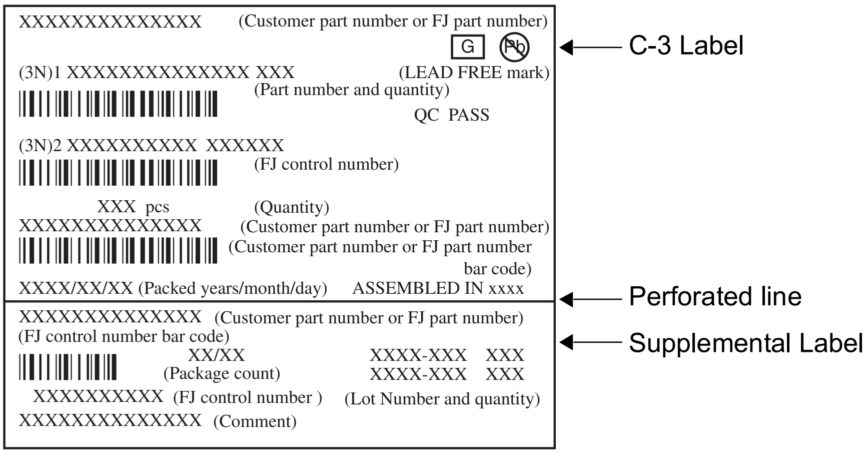

Reel cutout dimensions
A
B
C
W1
W2

Dimensions in mm

| A | B | C | W1 | W2 |
|---|---|---|---|---|
| 330 | 100 | 13 | 13.5 | 17.5 |

## 2.4 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



XXXXXXXXXXXXXX (Customer part number or FJ part number)

G Pb

(3N)1 XXXXXXXXXXXXXX XXX (LEAD FREE mark)

(Part number and quantity)

QC PASS

(3N)2 XXXXXXXXXX XXXXXX

(FJ control number)

XXX pcs (Quantity)

XXXXXXXXXXXXXX (Customer part number or FJ part number)

(Customer part number or FJ part number bar code)

XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx

XXXXXXXXXXXXXX (Customer part number or FJ part number)

(FJ control number bar code)

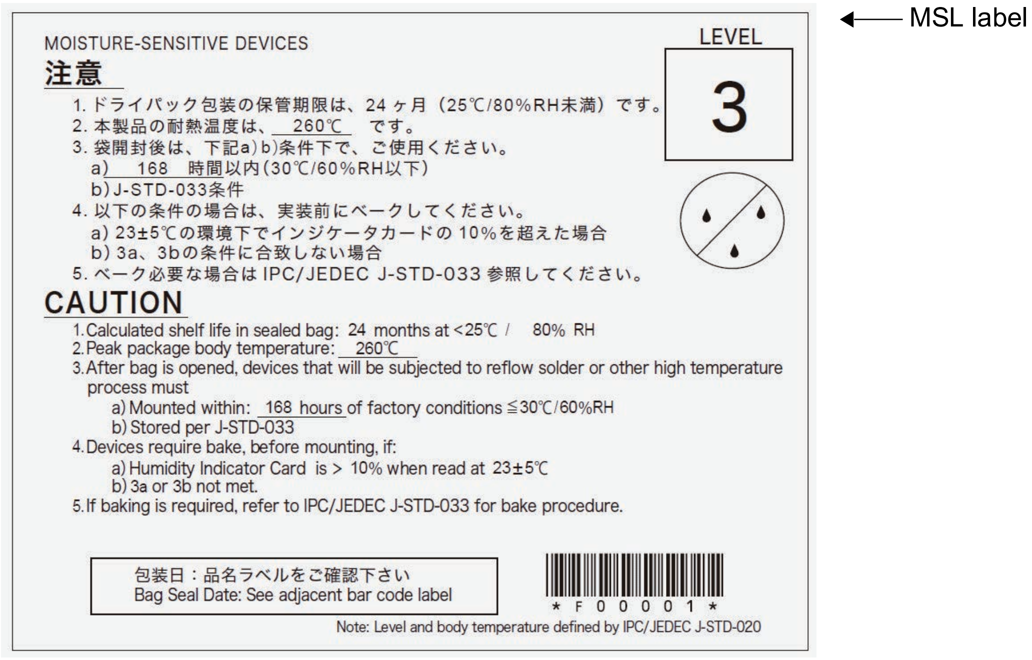
XX/XX (Package count)

XXXX-XXX XXX
XXXX-XXX XXX

XXXXXXXXXX (FJ control number ) (Lot Number and quantity)

XXXXXXXXXXXXXX (Comment)

Label II: Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)
[MSL Label (100mm × 70mm)]



MOISTURE-SENSITIVE DEVICES

LEVEL 3

注意

1. ドライパック包装の保管期限は、24ヶ月（25℃/80%RH未満）です。
2. 本製品の耐熱温度は、260℃ です。
3. 袋開封後は、下記a)b)条件下で、ご使用ください。
   - a) 168 時間以内(30℃/60%RH以下)
   - b) J-STD-033条件
4. 以下の条件の場合は、実装前にベークしてください。
   - a) 23±5℃の環境下でインジケータカードの 10%を超えた場合
   - b) 3a、3bの条件に合致しない場合
5. ベーク必要な場合は IPC/JEDEC J-STD-033 参照してください。

CAUTION

1. Calculated shelf life in sealed bag: 24 months at <25℃ / 80% RH
2. Peak package body temperature: 260℃
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   - a) Mounted within: 168 hours of factory conditions ≦30℃/60%RH
   - b) Stored per J-STD-033
4. Devices require bake, before mounting, if:
   - a) Humidity Indicator Card is > 10% when read at 23±5℃
   - b) 3a or 3b not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

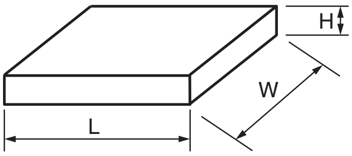
包装日：品名ラベルをご確認下さい
Bag Seal Date: See adjacent bar code label

* F 0 0 0 0 1 *

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

## 2.5 Dimensions for Containers

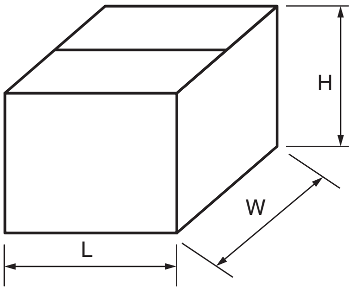
### (1) Dimensions for inner box



| L | W | H |
|---|---|---|
| 350 | 335 | 35 |

(Dimensions in mm)

### (2) Dimensions for outer box



| L | W | H |
|---|---|---|
| 384 | 368 | 225 |

(Dimensions in mm)

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

| Page | Section | Change Results |
|---|---|---|
| — | Overall | Following technical word is revised to more commonly used one.<br>FRAM to FeRAM |

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*https://ramxeed.com/*

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