Memory FeRAM

8 M (1024 K × 8) Bit Quad SPI

MB85RQ8MLX

■ DESCRIPTION

MB85RQ8MLX is a FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 1,048,576 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.
MB85RQ8MLX adopts the Quad Serial Peripheral Interface (QSPI) which can realize a high bandwidth such as Read and Write at 54 MB/s using four bi-directional pins (Quad I/O).
The MB85RQ8MLX is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MB85RQ8MLX can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^2PROM.
MB85RQ8MLX does not take long time to write data like Flash memories or E^2PROM.
MB85RQ8MLX is able to write data at a high bandwidth without any waiting time and fits perfectly into Networking, Gaming, Industrial computing, Camera, RAID controllers, etc.

■ FEATURES

- Bit configuration : 1,048,576 words × 8 bits
- Serial Peripheral Interface : SPI (Serial Peripheral Interface) / Dual SPI / Quad SPI
  Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Write supports : Single data input / Dual data input / Dual address and data input / Quad data input / Quad address and data input / DPI mode / QPI mode
- Read supports : Single data output / Fast single data output / Fast dual data out put / Fast dual data out put and data out put / Fast quad data output / Fast quad address input and data output / DPI mode / QPI mode / XIP mode
- Operating frequency : 108 MHz (Except normal READ command)
- High endurance : 10^{13} Read/Write per byte
- Data retention : 10 years (+105 °C), 95 years (+ 55 °C), over 200 years (+ 35 °C)
- Operating power supply voltage : 1.7 V to 1.95 V (Single power supply)
- Power consumption : Operating power supply current 18 mA (Max@Quad I/O 108 MHz)
  Standby current 30 μA (Typ), 180 μA (Max)
- Operation ambient temperature range : -40 °C to +105 °C
- Package : 16-pin plastic SOP
  RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited.
RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

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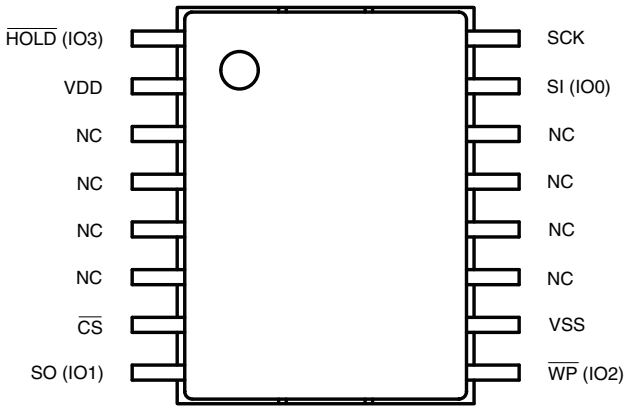
■ PIN ASSIGNMENT

(TOP VIEW)



(16-pin plastic SOP)

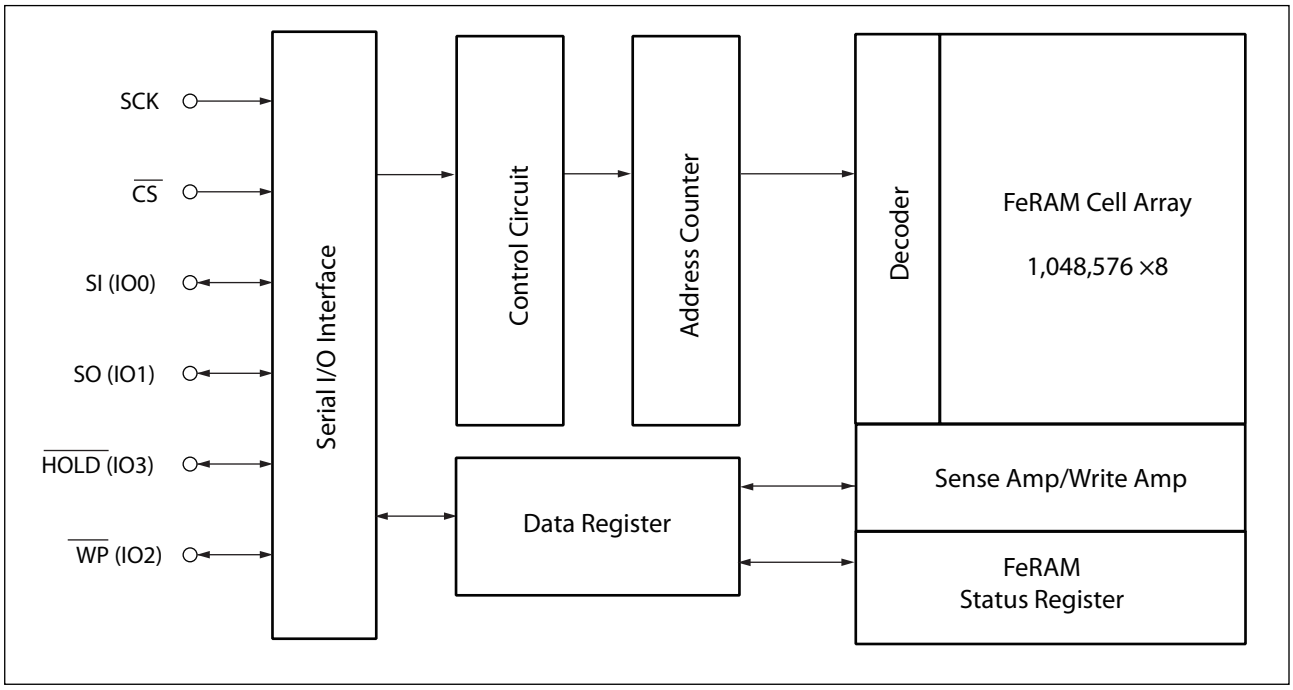
NC: Non connect pin

■ PIN FUNCTIONAL DESCRIPTIONS

Pin No.	Pin Name	Functional description
7	$\overline{CS}$	Chip Select pin This is an input pin to make chips select. When $\overline{CS}$ is “H” level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{CS}$ is “L” level, device is in select (active) status. $\overline{CS}$ has to be “L” level before inputting op-code.
9	$\overline{WP}$ (IO2)	Write Protect pin except in Quad SPI mode This is a pin to control writing to a status register. The writing of status register (see “■ STATUS REGISTER”) is protected in related with $\overline{WP}$ and WPEN bit of the status register. See “■ WRITING PROTECT” for detail. (Serial Data Input Output 2 in Quad SPI mode)
1	$\overline{HOLD}$ (IO3)	Hold pin except in Quad SPI mode This pin is used to interrupt serial input/output without making chips deselect. When $\overline{HOLD}$ is “L” level, hold operation is activated, SO becomes High-Z, SCK and SI become “don’t care”. See “■ HOLD OPERATION” for detail. (Serial Data Input Output 3 in Quad SPI mode)
16	SCK	Serial Clock pin This is a clock input pin to input/output serial data. Inputs data are latched synchronously to a rising edge, Outputs data occur synchronously to a falling edge.
15	SI (IO0)	Serial Data Input pin except in Dual SPI / Quad SPI mode This is an input pin of serial data. This inputs op-code, addresses and writing data. (Serial Data Input Output 0 in Dual SPI / Quad SPI mode)
8	SO (IO1)	Serial Data Output pin except in Dual SPI / Quad SPI mode This is an output pin of serial data. Reading data of FeRAM memory cell array and status register data are output. This is High-Z during standby. (Serial Data Input Output 1 in Dual SPI / Quad SPI mode)
2	VDD	Supply Voltage pin
10	VSS	Ground pin

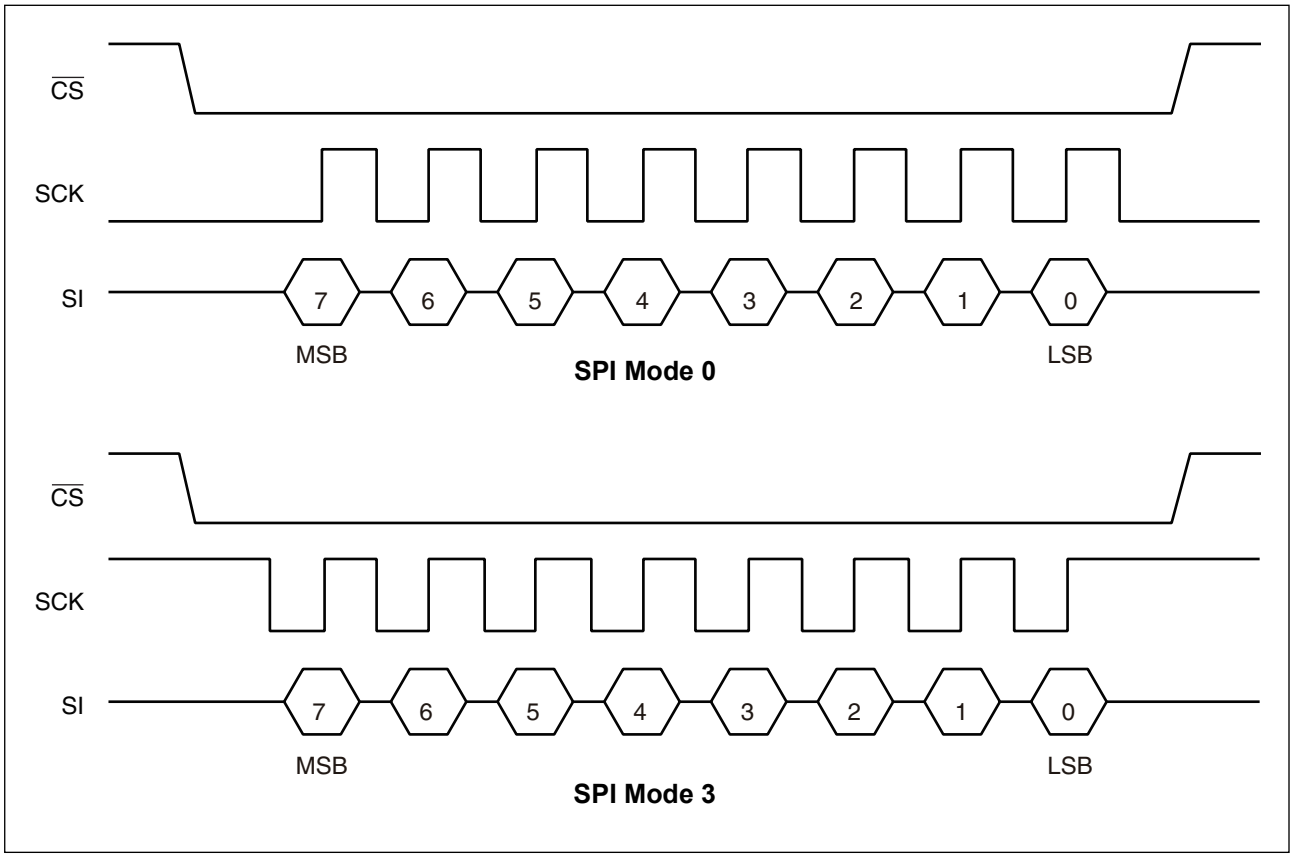
* When using Quad SPI mode instructions, the SI, SO, $\overline{WP}$ and $\overline{HOLD}$ pins become bidirectional IO0, IO1, IO2 and IO3 pins.

■ BLOCK DIAGRAM



■ SPI MODE

MB85RQ8MLX corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0) , and SPI mode 3 (CPOL = 1, CPHA = 1) .



■ SERIAL PERIPHERAL INTERFACE (SPI)

- **SPI**

  MB85RQ8MLX works as a slave of SPI. SPI uses the SI serial input pin to write op-code, addresses or data to the device on the rising edge of SCK. The SO serial output pin is used to read data or status register from the device on the falling edge of SCK.

- **Dual SPI**

  MB85RQ8MLX works as a slave of Dual SPI. MB85RQ8MLX supports Dual SPI mode using the “FRDO”, “FRDAD”, “WDD” and “WDAD” commands, DPI mode using the “EDPI” and “ESPI” commands and XIP mode. When using Dual SPI mode instructions, the SI and SO pins become bidirectional IO0 and IO1 pins respectively.

- **Quad SPI**

  MB85RQ8MLX works as a slave of Quad SPI. MB85RQ8MLX supports Quad SPI mode using the “FRQO”, “FRQAD”, “WQD” and “WQAD” commands, QPI mode using the “EQPI” and “ESPI” commands and XIP mode. When using Quad SPI mode instructions, the SI, SO, $\overline{WP}$ and $\overline{HOLD}$ pins become bidirectional IO0, IO1, IO2 and IO3 pins respectively.

■ STATUS REGISTER1

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memory (FeRAM). WPEN protects writing to a status register (refer to "■ WRITING PROTECT") relating with $\overline{WP}$ input. Writing with the WRSR command and reading with the RDSR command are possible.
6	QPI	QPI mode bit This is a volatile bit and "0" after power-on and defines QPI mode enabled/disabled. 1 = QPI mode enabled, set by the EQPI command 0 = QPI mode disabled, reset by the ESPI/EDPI command The QPI bit cannot be changed with the WRSR command. Reading with the RDSR command is possible. Both of the QIP bit contents are the same of status register1 and status register2.
5	LC1	LC (Latency Control) mode bit These are bits composed of nonvolatile memories. These define number of dummy cycles for the FRDO, FRDAD, FRQO and FRQAD commands (refer to "■ LC Mode"). Writing with the WRSR command and reading with the RDSR command are possible.
4	LC0	
3	BP1	Block Protect These are bits composed of nonvolatile memories. These define size of write protect block for the WRITE, WDD, WDAD, WQD and WQAD commands (refer to "■ BLOCK PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This is a volatile bit and "0" after power-on and indicates FeRAM Array and status register are writable. 1 = writable, set by the WREN command 0 = unwritable, reset by the WRDI command With the RDSR command, reading is possible but writing is impossible with the WRSR command. WEL is reset after the following operations. After power-on. After the WRDI command recognition. Achieving continuous writing mode, WEL is not reset after following operations making it possible to execute writing commands continuously. WRSR command WRITE command WDD command WDAD command WQD command WQAD command
0	0	This is a bit fixed to "0".

■ STATUS REGISTER2

Bit No.	Bit Name	Function
7	RFU	This is a bit fixed to “0”.
6	QPI	QPI mode bit This is a volatile bit and “0” after power-on and defines QPI mode enabled/disabled. 1 = QPI mode enabled, set by the EQPI command 0 = QPI mode disabled, reset by the ESPI/EDPI command Reading with the RDSR2 command is possible. Both of the QIP bit contents are the same of status register1 and status register2.
5	DPI	DPI mode bit This is a volatile bit and “0” after power-on and defines DPI mode enabled/disabled. 1 = DPI mode enabled, set by the EDPI command 0 = DPI mode disabled, reset by the ESPI/EQPI command Reading with the RDSR2 command is possible.
4	RFU	This is a bit fixed to “0”.
3	RFU	This is a bit fixed to “0”.
2	RFU	This is a bit fixed to “0”.
1	RFU	This is a bit fixed to “0”.
0	RFU	This is a bit fixed to “0”.

■ OP-CODE

MB85RQ8MLX accepts 10 kinds of SPI Mode command, 4 kinds of Dual SPI Mode command and 4 kinds of Quad SPI Mode command and 3 kinds of mode switching command, specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If $\overline{CS}$ is risen while inputting op-code, the command are not performed.

Mode	Name	Description	Op-code	Max Freq. (MHz)	DDPI /PI	QPI	XIP	LC
SPI	WREN	Set Write Enable Latch	0000 0110B	108	Yes	Yes	No	No
	WRDI	Reset Write Enable Latch	0000 0100B	108	Yes	Yes	No	No
	RDSR	Read Status Register1	0000 0101B	108	Yes	Yes	No	No
	WRSR	Write Status Register1	0000 0001B	108	Yes	Yes	No	No
	RDSR2	Read Status Register2	0011 0101B	108	Yes	Yes	No	No
	READ	Read	0000 0011B	40	No	No	No	No
	WRITE	Write	0000 0010B	108	No	No	No	No
	RDID	Read Device ID	1001 1111B	108	Yes	Yes	No	No
	RUID	Read Unique ID	0100 1100B	108	No	No	No	No
	FSTRD	Fast Read Memory Code	0000 1011B	108	No	No	Yes	Yes
Dual SPI	FRDO	Fast Read Dual Output	0011 1011B	108*	Yes	No	Yes	Yes
	FRDAD	Fast Read Dual Address and Data	1011 1011B	108*	Yes	No	Yes	Yes
	WDD	Write Dual Data	1010 0010B	108	Yes	No	No	No
	WDAD	Write Dual Address and Data	1010 0001B	108	Yes	No	No	No
Quad SPI	FRQO	Fast Read Quad Output	0110 1011B	108*	No	Yes	Yes	Yes
	FRQAD	Fast Read Quad Address and Data	1110 1011B	108*	No	Yes	Yes	Yes
	WQD	Write Quad Data	0011 0010B	108	No	Yes	No	No
	WQAD	Write Quad Address and Data	0001 0010B	108	No	Yes	No	No
Mode Switch -ing	EDPI	Enable DPI mode	0011 0111B	108	No	Yes	No	No
	EQPI	Enable QPI mode	0011 1000B	108	Yes	No	No	No
	ESPI	Disable DPI/QPI mode	1111 1111B	108	Yes	Yes	No	No

*: The frequency when the number of dummy cycles is the maximum value. (see "■ LC MODE").

Notes

1. "Yes": Commands are supported in this mode, "No": Commands are not supported.
2. FRQAD command cannot be issued as 1st command after power-on. Any other command shall be issued at least once before FRQAD command.

3-1. Single Input Address (3bytes)
SI= X, X, X, X, A19, A18, A17, A16, A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0
(Upper 4bit = any)

3-2. Dual Input Address (3bytes)
IO0=X, X, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0
IO1=X, X, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1
(Upper 4bit = any)

3-3. Quad Input Address (3bytes)
IO0=X, A16, A12, A8, A4, A0
IO1=X, A17, A13, A9, A5, A1
IO2=X, A18, A14, A10, A6, A2
IO3=X, A19, A15, A11, A7, A3

(Upper 4bit = any)

4-1. Single I/O Data

SI (or SO)=D7, D6, D5, D4, D3, D2, D1, D0

4-2. Dual Data

IO0=D6,D4, D2, D0

IO1=D7,D5, D3, D1

4-3. Quad Data

IO0=D4, D0

IO1=D5, D1

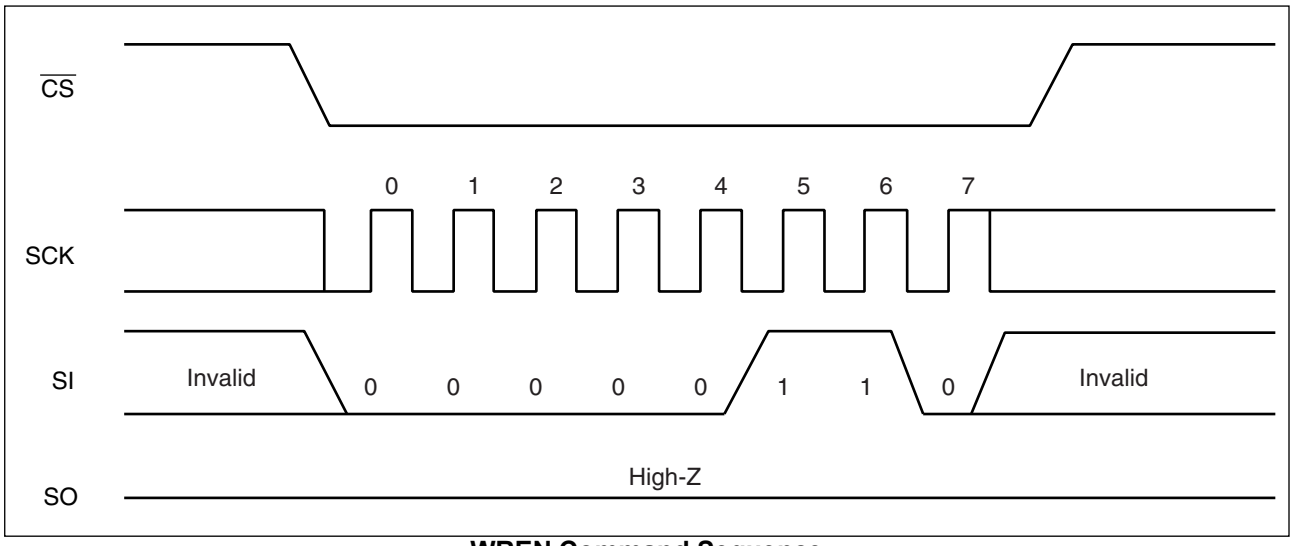
IO2=D6, D2

IO3=D7, D3

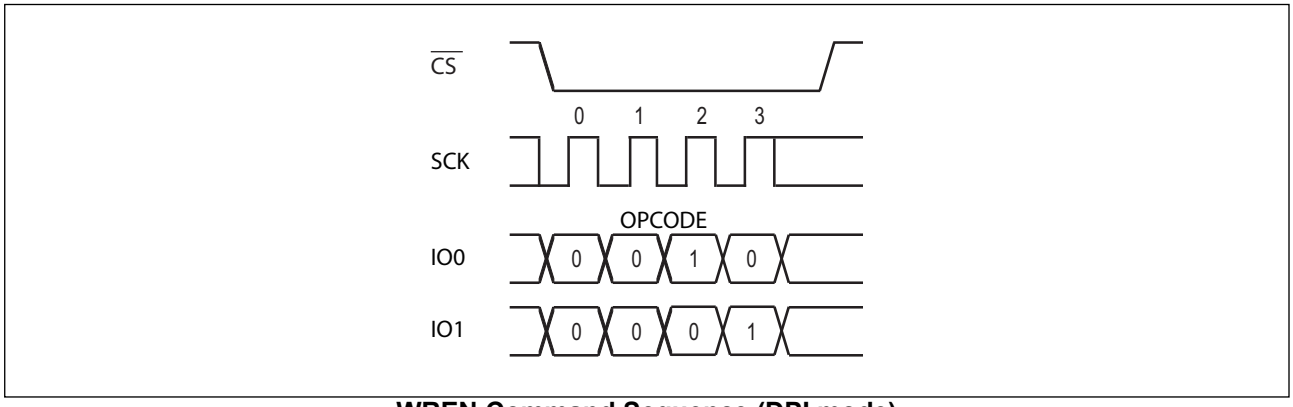
■ COMMAND

• WREN

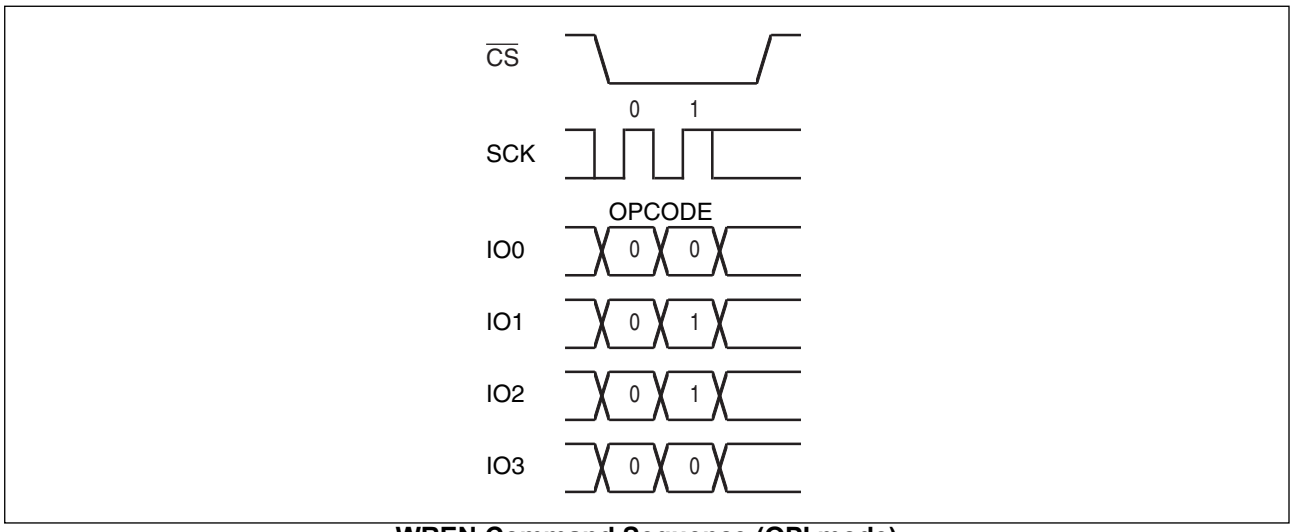
The WREN command sets WEL (Write Enable Latch) . WEL has to be set with the WREN command before writing operation (WRSR, WRITE, WDD, WDAD, WQD and WQAD commands) . The maximum clock frequency for the WREN command is 108 MHz.



WREN Command Sequence



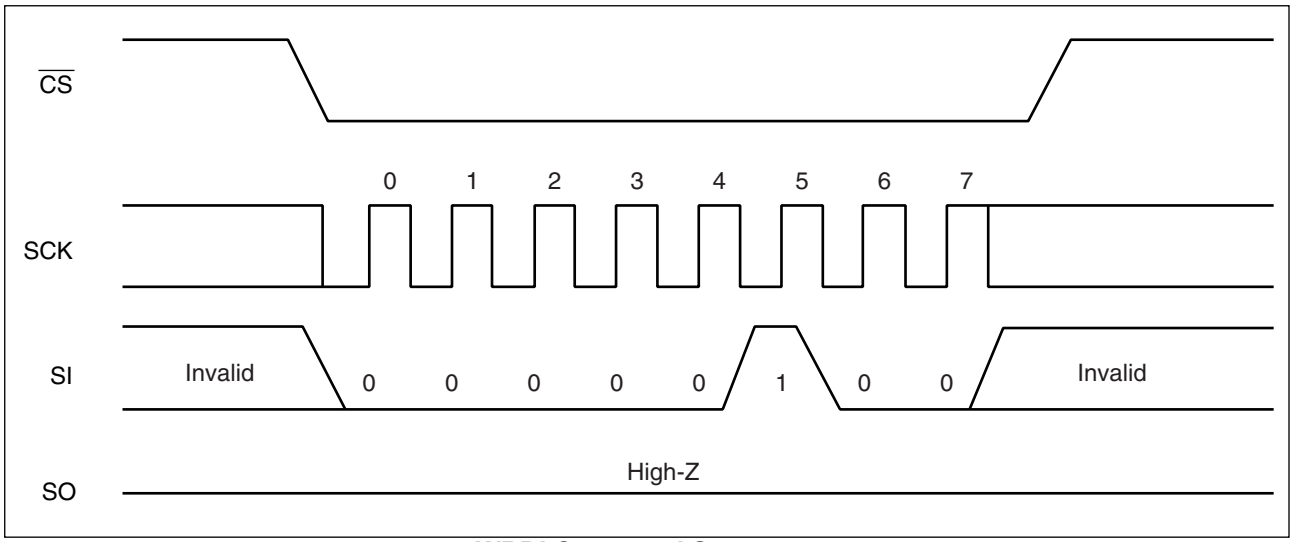
WREN Command Sequence (DPI mode)



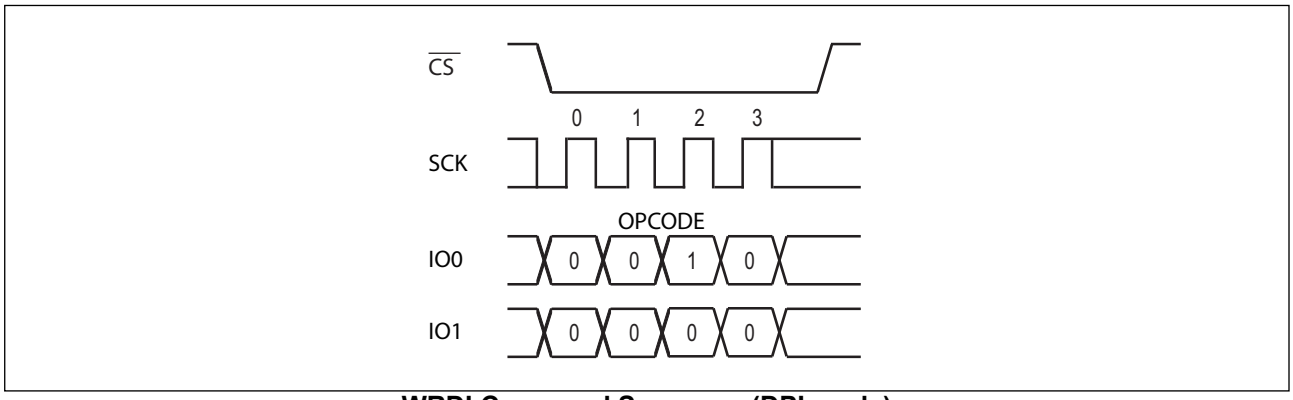
WREN Command Sequence (QPI mode)

• **WRDI**

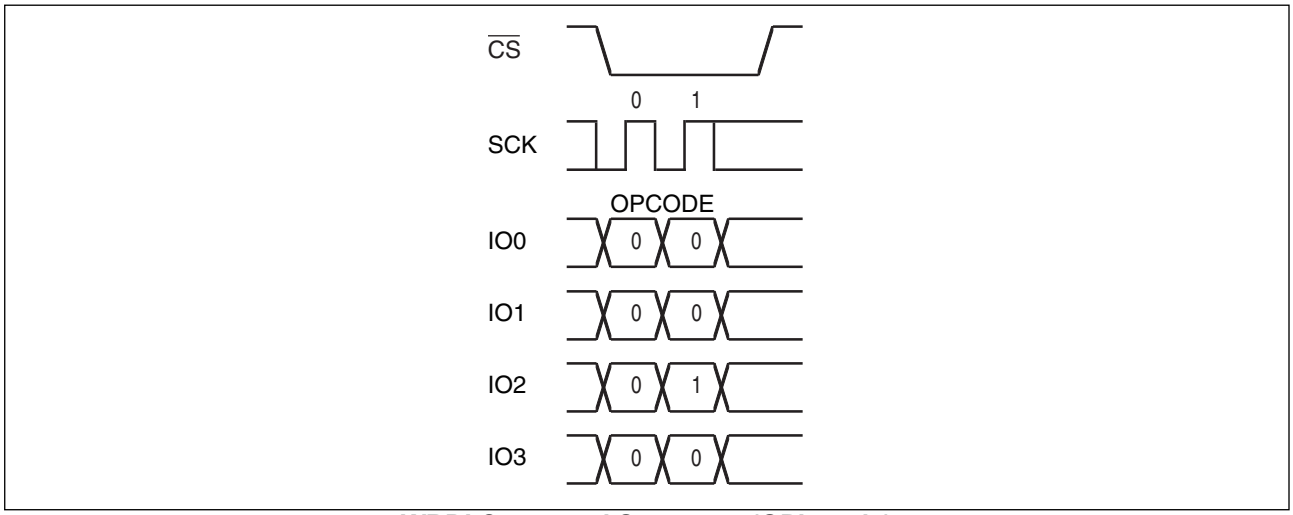
The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRSR, WRITE, WDD, WDAD, WQD and WQAD commands) are not performed when WEL is reset. The maximum clock frequency for the WRDI command is 108 MHz.



WRDI Command Sequence



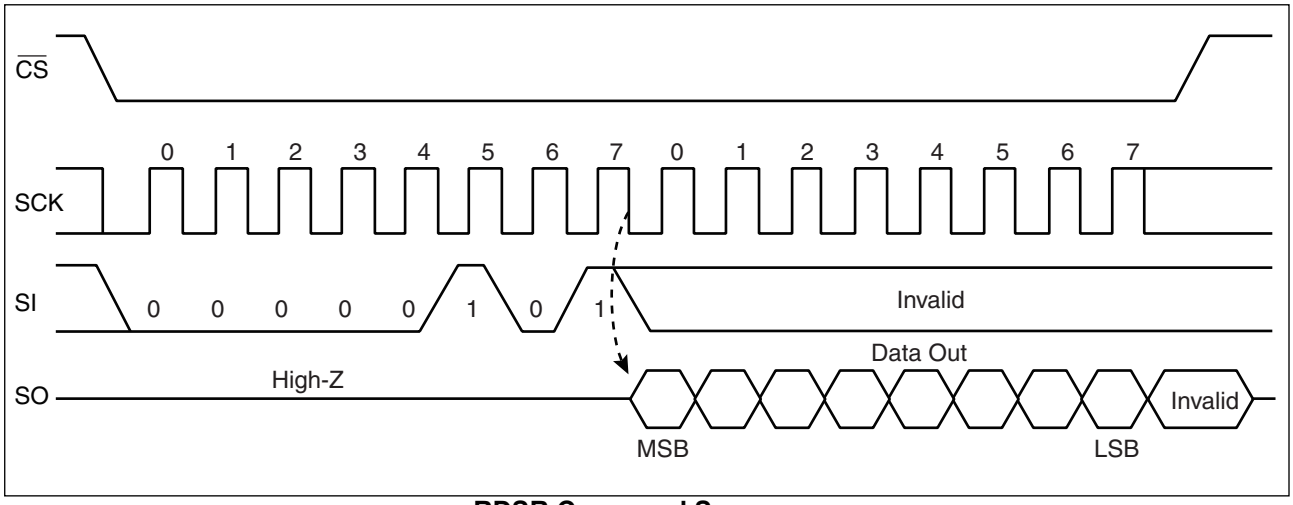
WRDI Command Sequence (DPI mode)



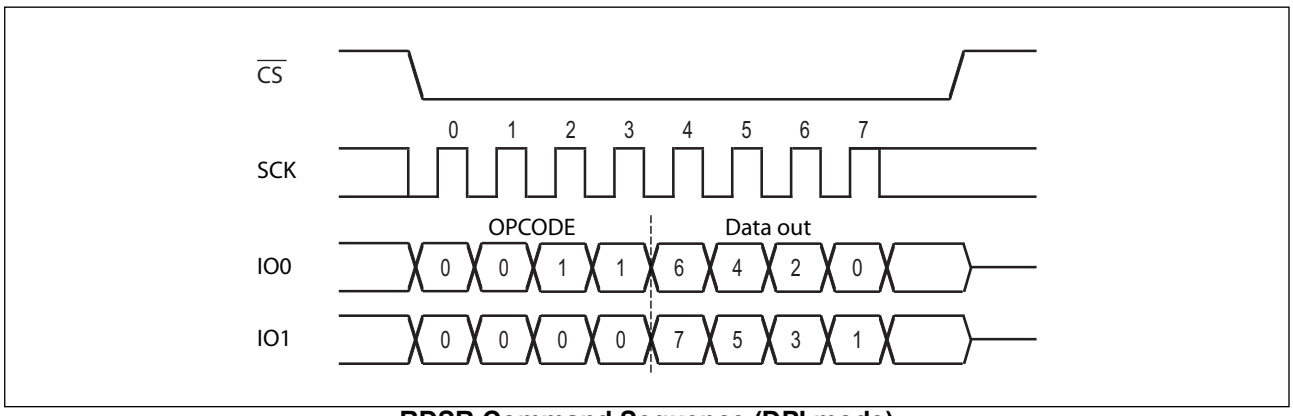
WRDI Command Sequence (QPI mode)

- **RDSR**

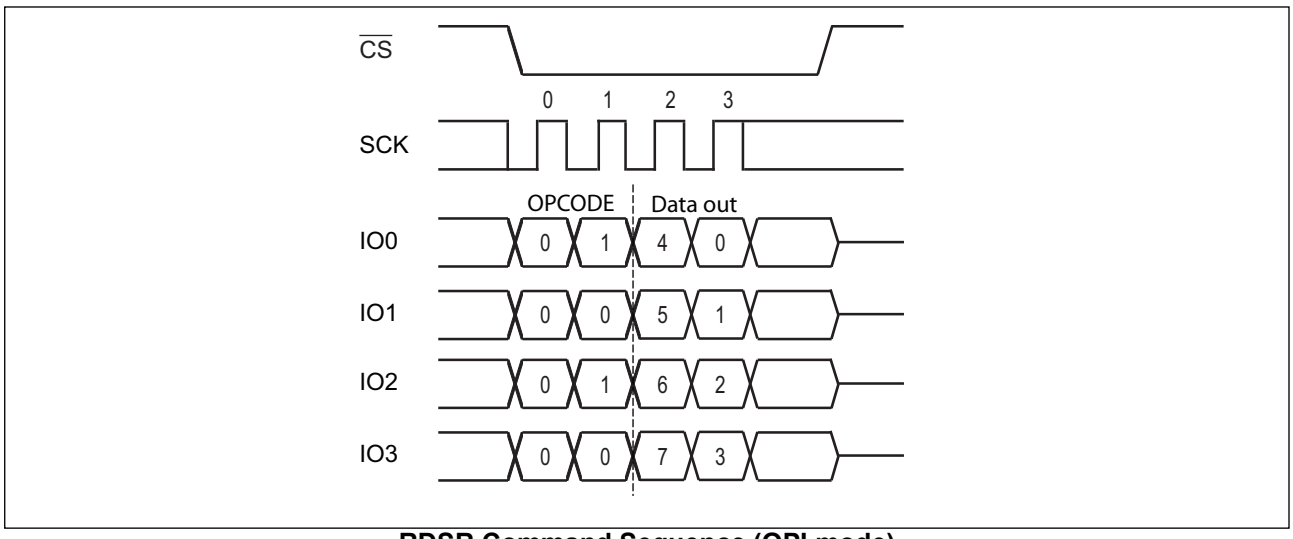
  The RDSR command reads status register1 data. After driving $\overline{CS}$ low, op-code of RDSR is input to SI and more 8-cycle clock is input to SCK, and then driving $\overline{CS}$ high. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of $\overline{CS}$. The maximum clock frequency for the RDSR command is 108 MHz.



RDSR Command Sequence



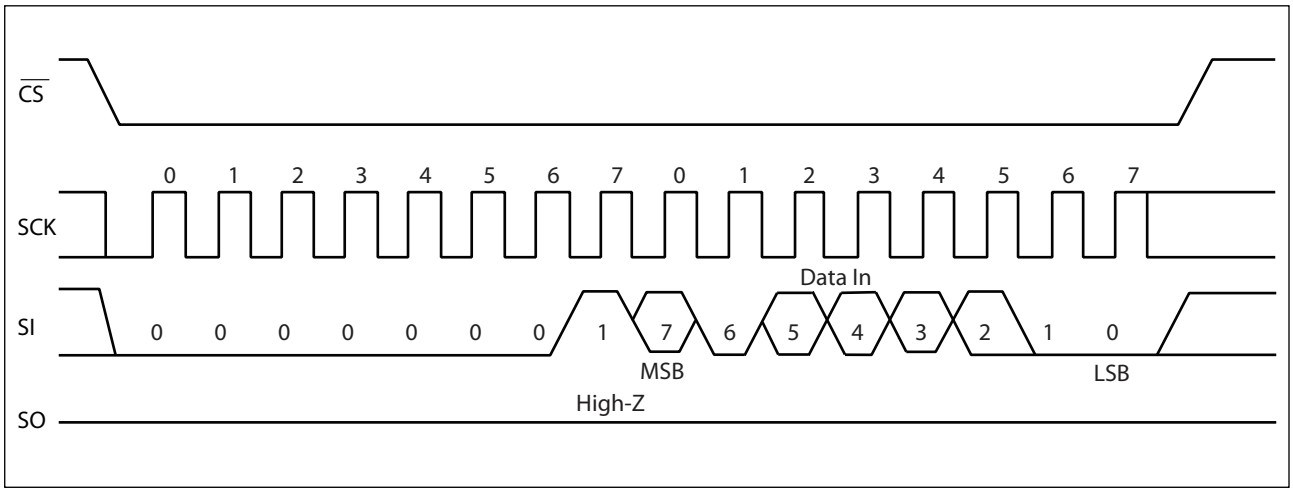
RDSR Command Sequence (DPI mode)



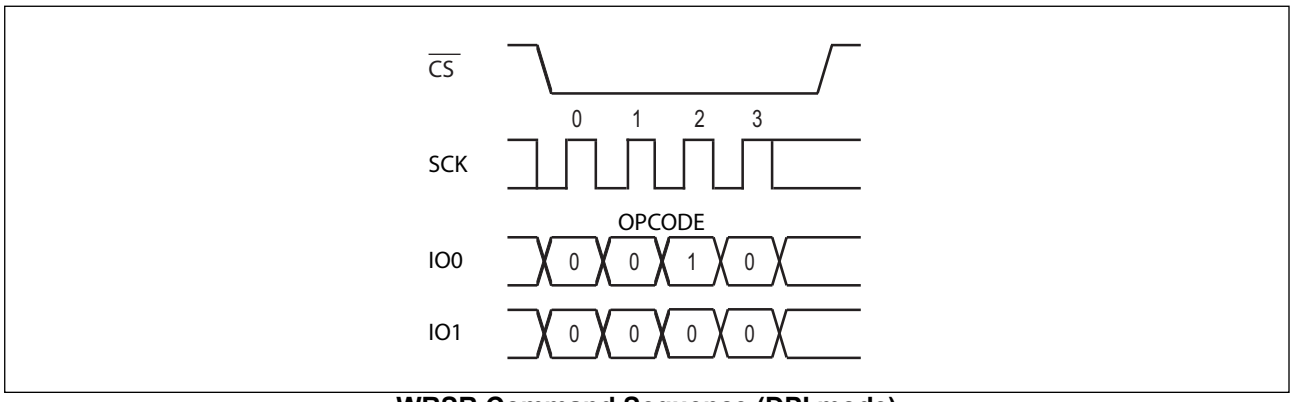
RDSR Command Sequence (QPI mode)

- **WRSR**

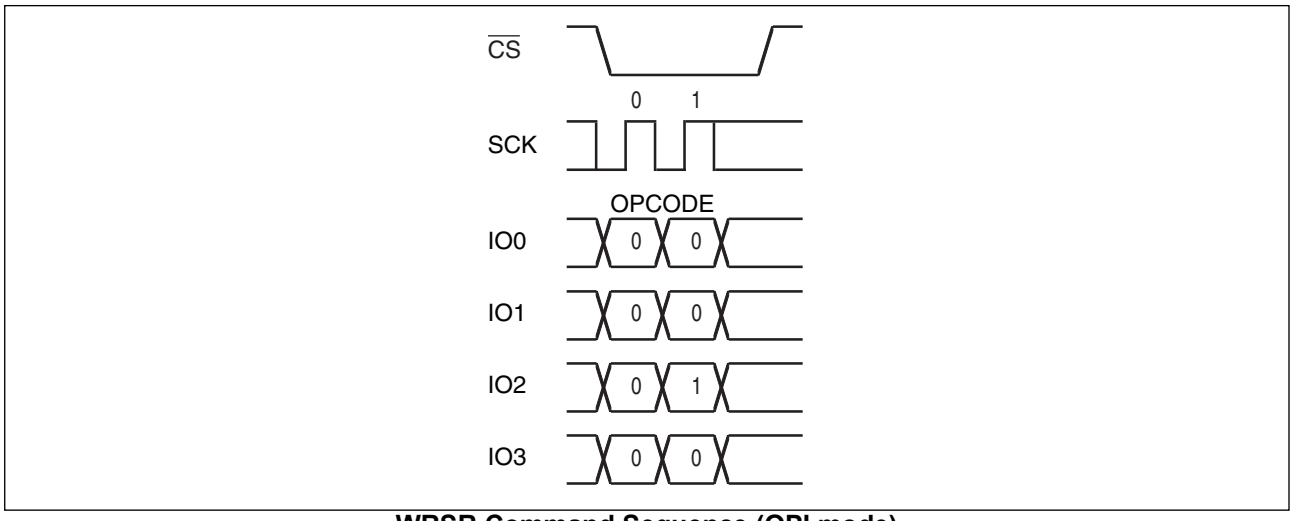
The WRSR command writes data to the nonvolatile memory bit of status register1. After driving $\overline{CS}$ low, op-code of WRSR and 8 writing data bits are input to SI, and then driving $\overline{CS}$ high. QPI mode bit is not able to be written with WRSR command. A SI value corresponding to bit 6 is ignored. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to “0” and cannot be written. The SI value corresponding to bit 0 is ignored. The $\overline{WP}$ signal level shall be fixed before performing WRSR command, and not be changed until the end of command sequence. The maximum clock frequency for the WRSR command is 108 MHz.



WRSR Command Sequence



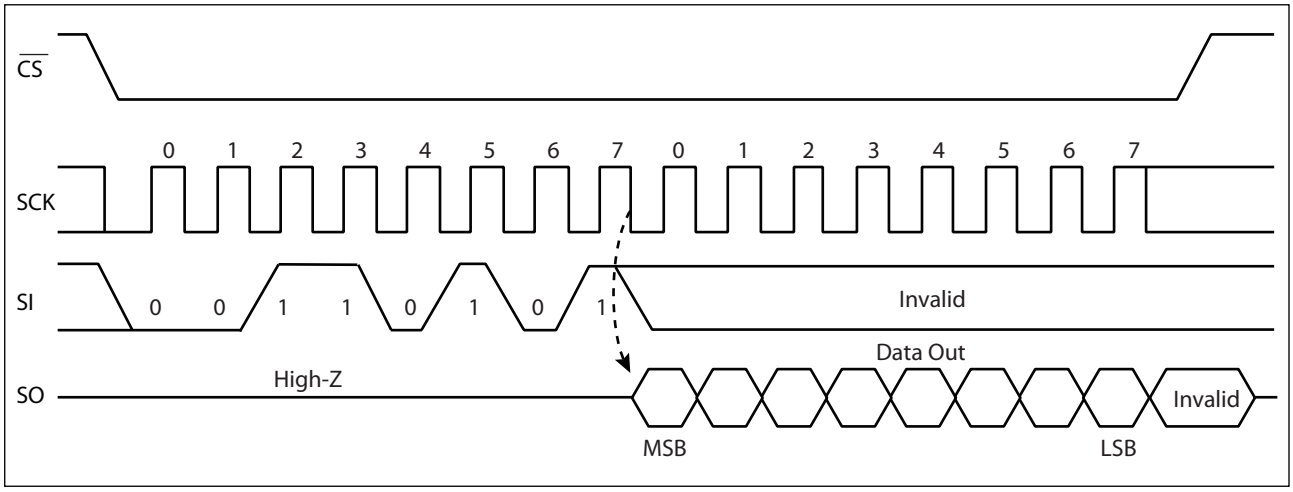
WRSR Command Sequence (DPI mode)



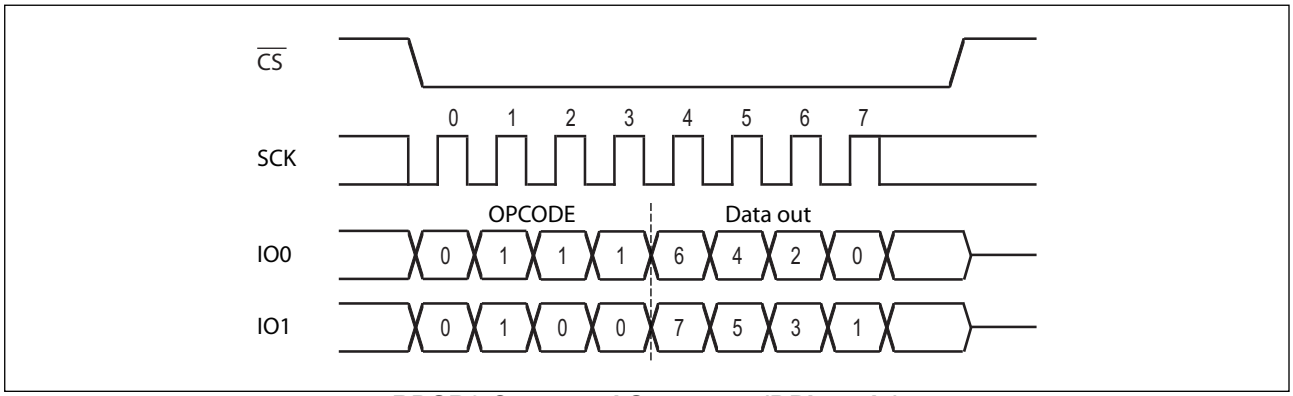
WRSR Command Sequence (QPI mode)

- **RDSR2**

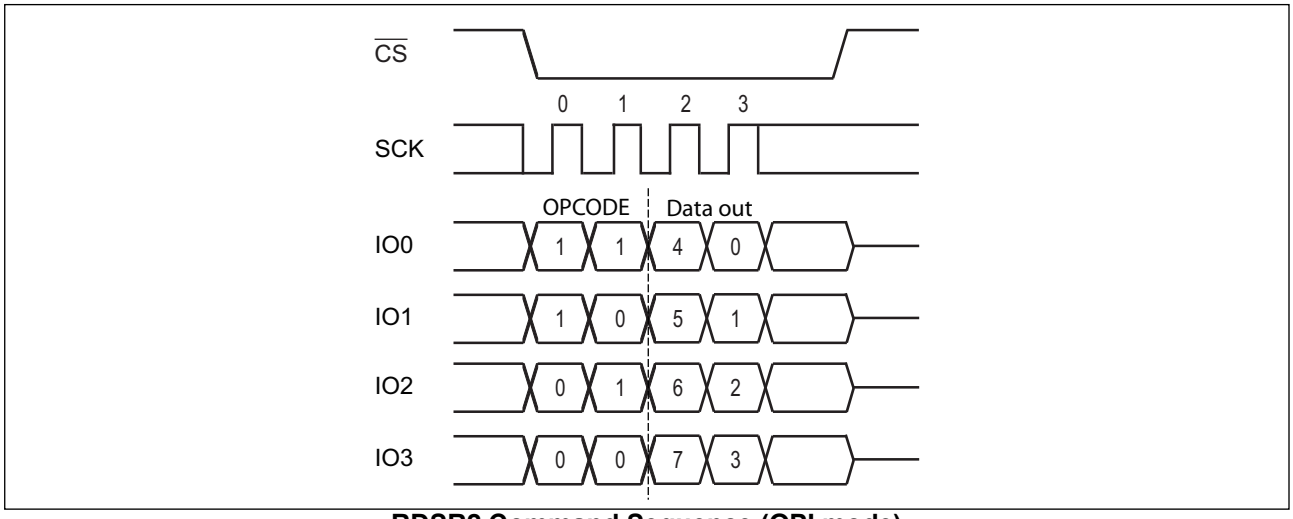
  The RDSR2 command reads data status register2. After driving $\overline{CS}$ low, RDSR2 op-code is input to SI and more 8 clock cycles are input to SCK, and then driving $\overline{CS}$ high. The SI value is invalid during this time. SO is output synchronously to a falling edge of SCK. When $\overline{CS}$ is risen, the RDSR2 command is completed, otherwise it keeps on reading from status register2 repeatedly which is enabled by continuously sending clocks to SCK before $\overline{CS}$ rising. The maximum clock frequency for the RDSR2 command is 108 MHz.



RDSR2 Command Sequence



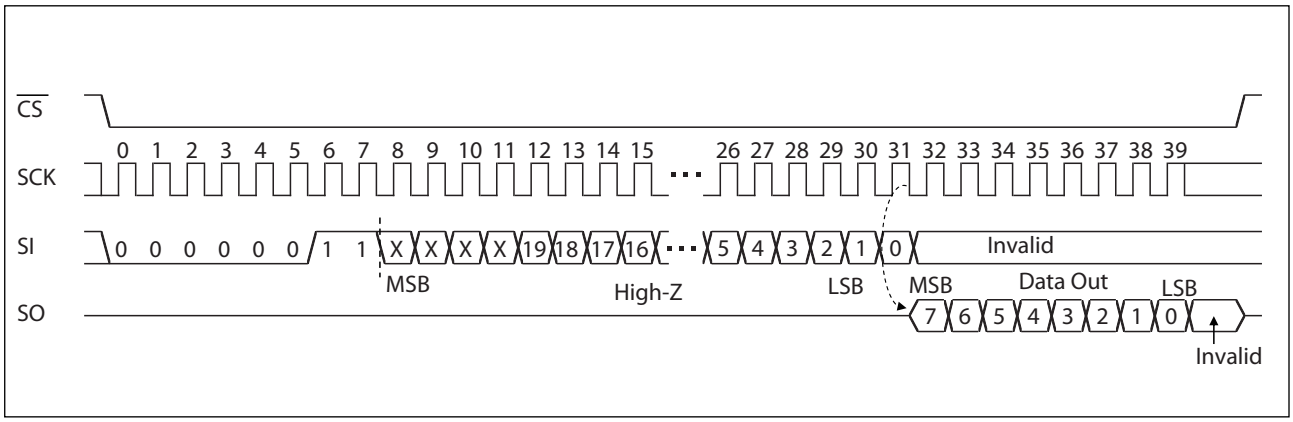
RDSR2 Command Sequence (DPI mode)



RDSR2 Command Sequence (QPI mode)

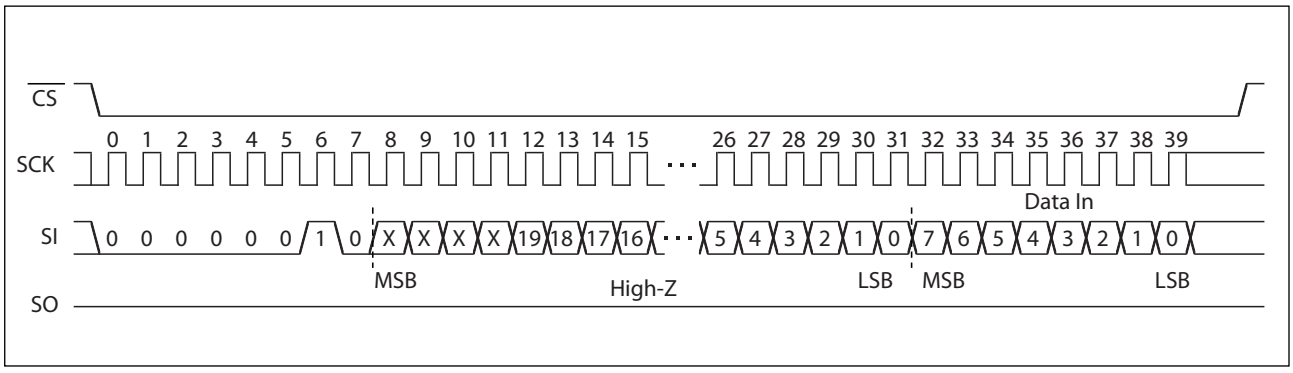
- **READ**

The READ command reads FeRAM memory cell array data. After driving $\overline{CS}$ low, READ op-code and arbitrary 24 address bits are input to SI. The 4 upper address bits are ignored. Then, 8 clock cycles are input to SCK. SO outputs 8 data bits synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the READ command is completed, otherwise it keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely. The maximum clock frequency for the READ command is 40 MHz.



- **WRITE**

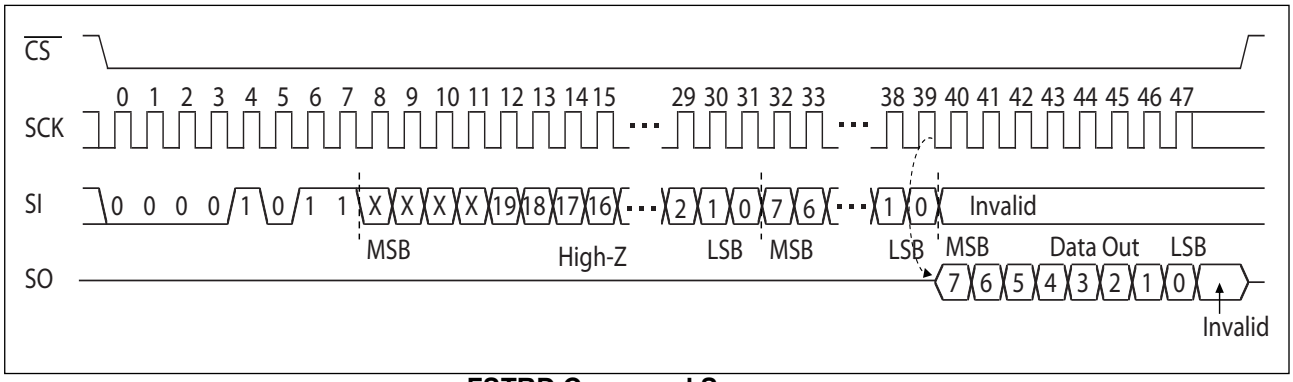
The WRITE command writes data to FeRAM memory cell array. After driving $\overline{CS}$ low, WRITE op-code, arbitrary 24 address bits and 8 writing data bits are input to SI. The 4-bit upper address bits are ignored. When 8 writing data bits are input, data is written to FeRAM memory cell array. Risen $\overline{CS}$ will terminate the WRITE command. However, if you continue sending the writing data for 8 bits each before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle keeps on infinitely. The maximum clock frequency for the WRITE command is 108 MHz.



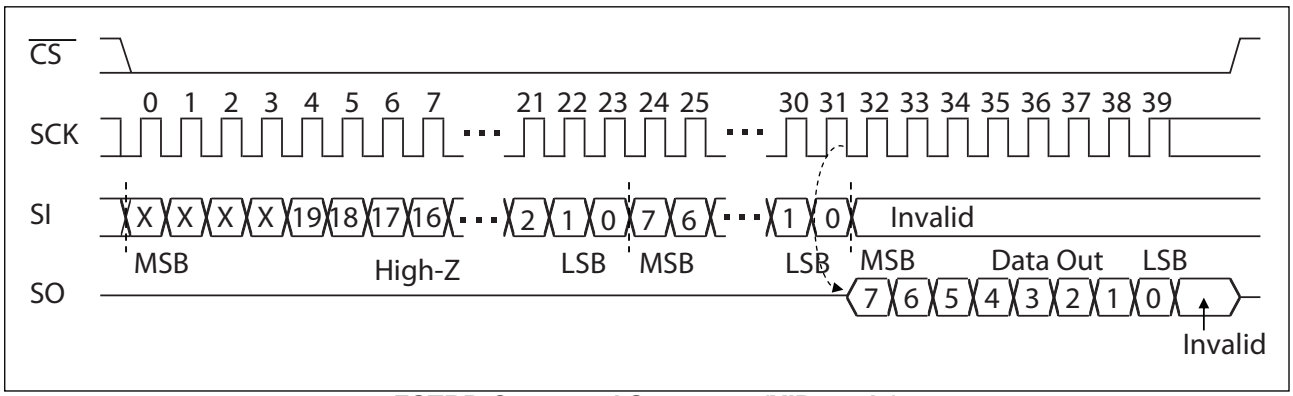
- **FSTRD**

The FSTRD command reads FeRAM memory cell array data. After driving $\overline{CS}$ low, FSTRD op-code and a arbitrary 24 address bits are input to SI, followed by 8 mode bits. The 4 upper address bits are ignored. Then, 8 clock cycles are input to SCK. SO outputs 8 data bits synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the FSTRD command is completed, otherwise it keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely. The maximum clock frequency for the FSTRD command is 108 MHz.

Address jumps can be done without the need for additional FSTRD command. This is controlled through the setting of the Mode bits after the address sequence. This added feature, which is called “XIP mode”, removes the need for the command sequence. If the Mode bits equal EF_H or AF_H, then the device remains in FSTRD mode and the next address can be entered (after $\overline{CS}$ is raised high and then asserted low) without requiring the FSTRD command, thus eliminating 8 cycles for the command sequence. If the Mode bits are any value other than EF_H and AF_H, then the next time $\overline{CS}$ is raised high the device will be released from FSTRD mode. After that, the device can accept SPI commands. $\overline{CS}$ should not be driven high during mode bits as this may make the mode bits indeterminate.



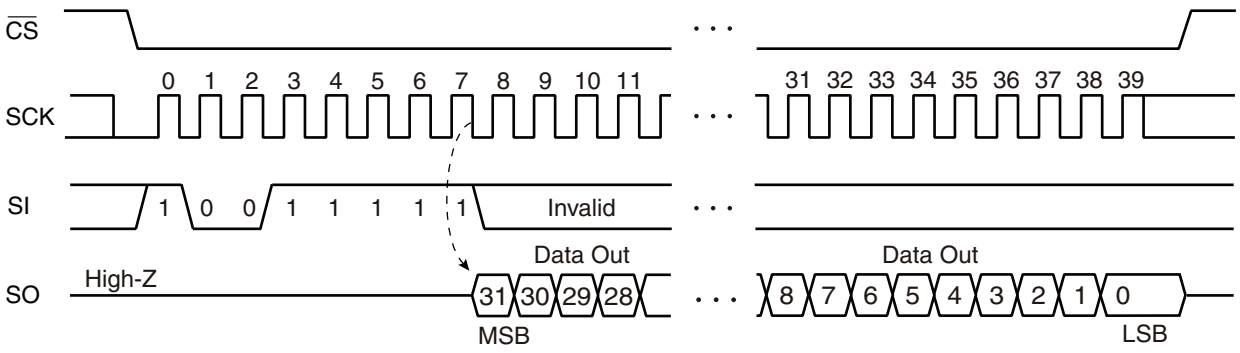
FSTRD Command Sequence



FSTRD Command Sequence (XIP mode)

- **RDID**

The RDID command reads fixed Device ID. After driving $\overline{CS}$ low, RDID op-code is input to SI and more 32 clock cycles are input to SCK, and then driving $\overline{CS}$ high. The SI value is invalid during this time. SO is output synchronously to a falling edge of SCK. The output order is: Manufacturer ID (8bit)/Continuation code (8bit)/ Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, SO holds the output state of the last bit in 32-bit Device ID until $\overline{CS}$ is risen. The maximum clock frequency for the RDID command is 108 MHz.

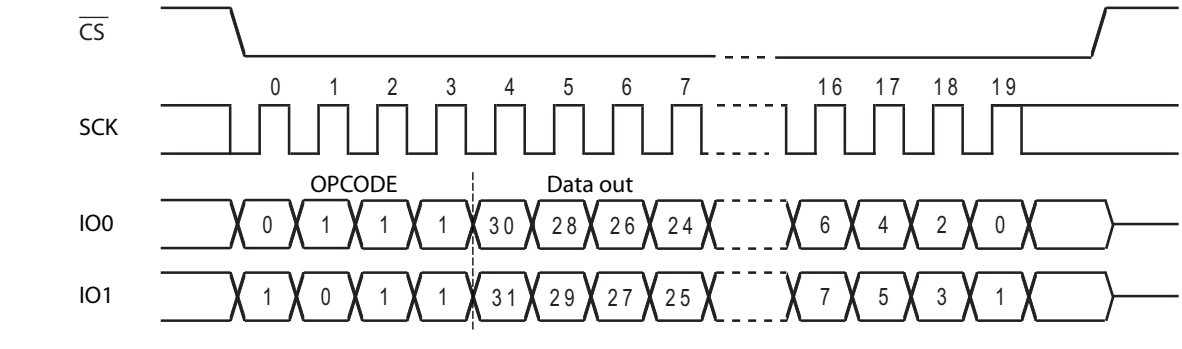


	bit									
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Hex**	
Manufacturer ID	0	0	0	0	0	1	0	0	04_H	Fujitsu
Continuation code	0	1	1	1	1	1	1	1	$7F_H$	

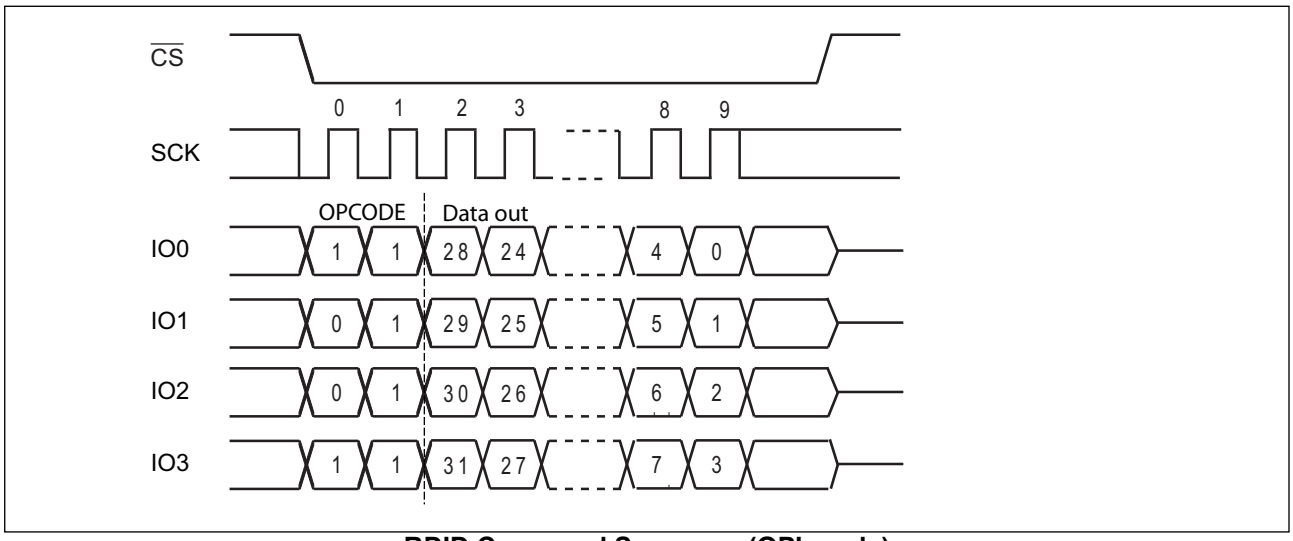
	Proprietary use			**Density**					**Hex**	
Product ID (1st Byte)	0	1	0	0	1	0	1	0	$4A_H$	Density: $01010_B = 8$ Mbit

	Proprietary use								**Hex**	
Product ID (2nd Byte)	1	0	0	0	0	1	0	1	85_H	

RDID Command Sequence



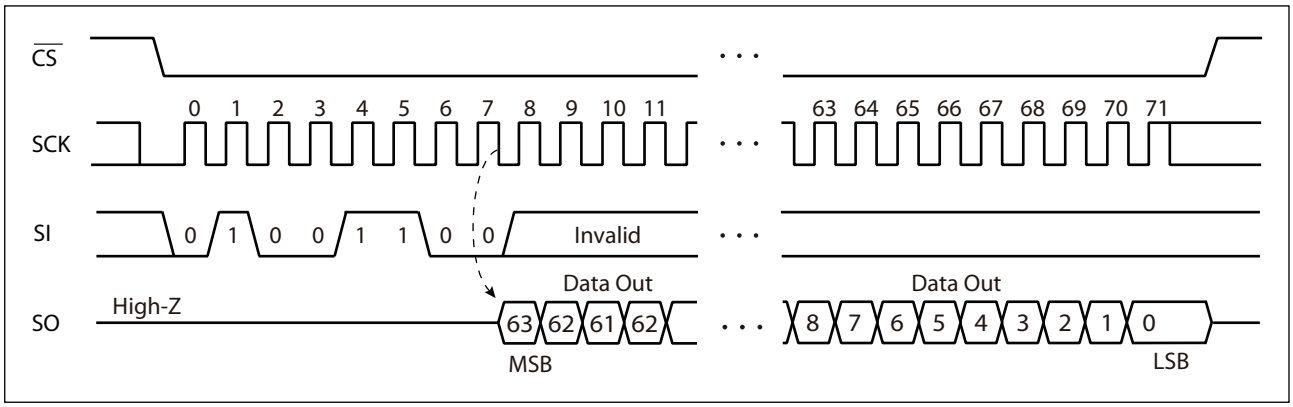
RDID Command Sequence (DPI)



RDID Command Sequence (QPI mode)

• **RUID**

The RUID command reads unique ID (64 bits) which is corresponding to each device. Op-code of RUID is input to SI and more 64-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The maximum clock frequency for the RUID command is 108 MHz.



RUID Command Sequence

■ LC MODE

The following read commands have a variable latency period between the end of mode bit and the beginning of read data.

- FRDO
- FRDAD
- FRQO
- FRQAD

This nonvolatile configuration bit (LC1, LC0) sets the number of dummy cycles(= latency period) to be used in advance, therefore MB85RQ8MLX can start to read immediately with an appropriate dummy cycles.

Dummy Cycles vs. SCK Frequency

LC1	LC0	FRDO,FRDAD command		FRQO, FRQAD command	
		Number of Dummy Cycles	Frequency Limit of SCK (MHz)	Number of Dummy Cycles	Frequency Limit of SCK (MHz)
0	0	4	108	6	108
0	1	2	78	4	78
1	0	0	46	2	46
1	1	0	46	0	15

*:the number in the parenthesis in “Number of Dummy Cycles” is added number of clock counts of mode bit.

■ DUAL SPI MODE COMMAND

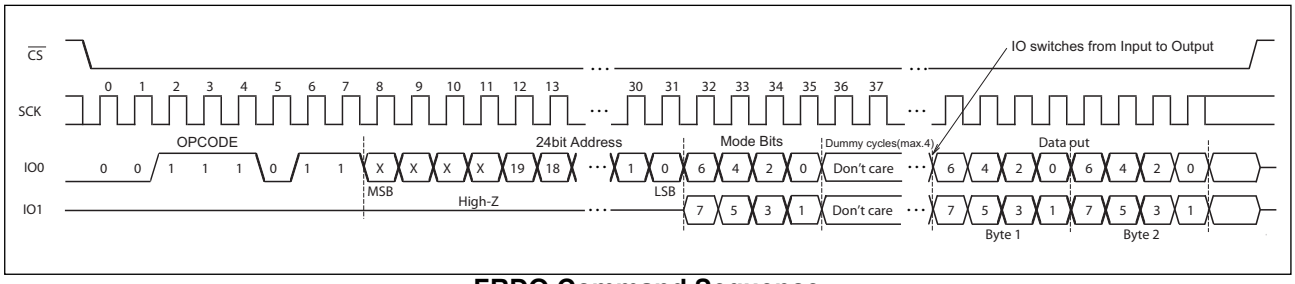
• FRDO (Fast Read Dual Output)

The FRDO command is similar to the FSTRD command, except that the data is shifted out 2 bits at one time using 2 I/O pins IO0 (SI) and IO1 (SO), at a maximum frequency of 108 MHz. The data transfer rate of the FRDO command is two times higher than the FSTRD command.

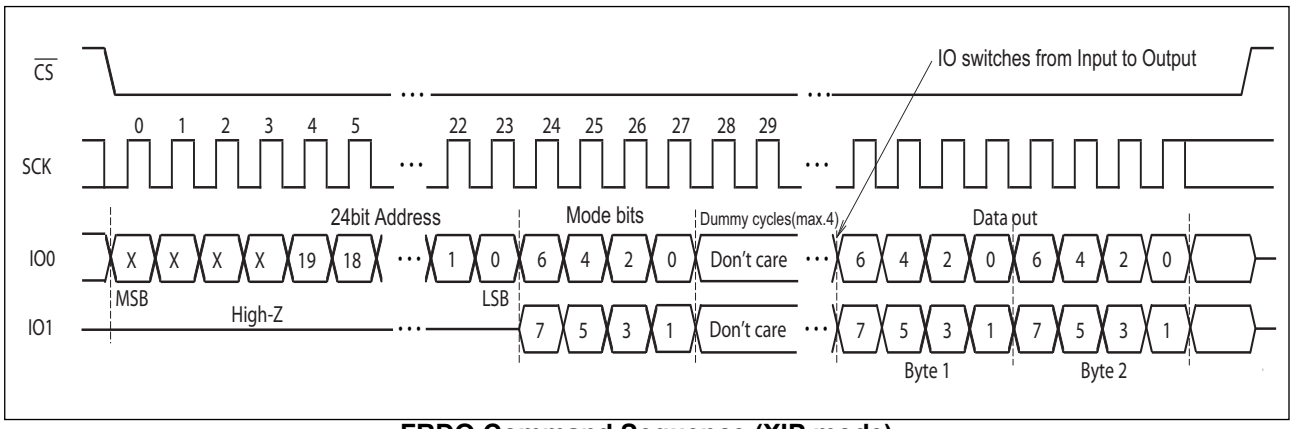
After driving $\overline{CS}$ low, FRDO op-code and arbitrary 24 address bits are input to IO0. The 4 upper address bits are ignored. Then mode bits are input to 2 I/O pins for 4 cycles, followed by dummy cycles. The number of dummy cycles is defined beforehand by the frequency of SCK, and configured by the latency bit of LC1 and LC0. The op-code, the address and the mode bits are latched on the rising edge of SCK. After that, FeRAM memory cell array data are shifted out 2 bits at one time through 2 I/O pins synchronously to the falling edge of SCK. When $\overline{CS}$ is risen, the FRDO command is completed, otherwise it keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 4 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.

Address jumps can be done without the need for additional FRDO command. This is controlled through the setting of the mode bits after the address sequence. This added feature, which is called “XIP mode”, removes the need for the command sequence. If the mode bits equal EF_H or AF_H, then the device remains in FRDO mode and the next address can be entered (after $\overline{CS}$ is raised high and then asserted low) without requiring the FRDO command, thus eliminating 8 cycles for the command sequence. If the mode bits are any value other than EF_H and AF_H, then the next time $\overline{CS}$ is raised high the device will be released from FRDO mode. After that, the device can accept SPI commands. $\overline{CS}$ should not be driven high during mode or dummy bits as this may make the mode bits indeterminate.

It is important that the I/O pins are set to high-impedance prior to the falling edge of the first data out clock. The FRDO command is terminated by driving $\overline{CS}$ high at any time during data output.



FRDO Command Sequence



FRDO Command Sequence (XIP mode)

- **FRDAD (Fast Read Dual Address and Data)**

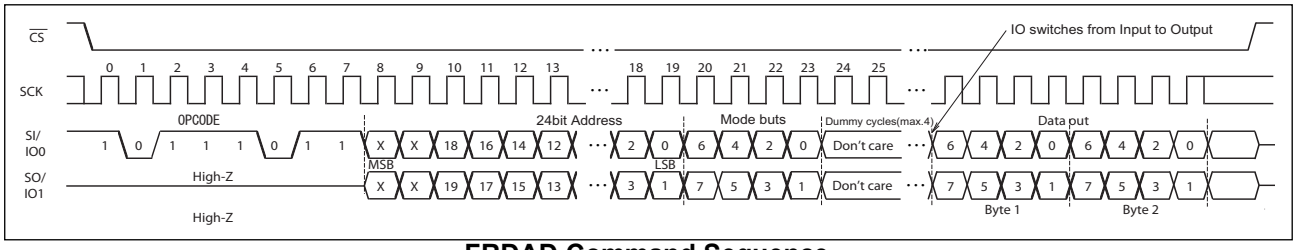
  The FRDAD command is similar to the FRDO command, except that it further improves throughput by allowing input of the address bits (A23-A0) using 2 bits per SCK via 2 I/O pins (IO0 (SI) and, IO1 (SO)), at a maximum frequency of 108 MHz.

  After driving $\overline{CS}$ low, FRDAD op-code is input to IO0. Then 24 address bits and 8 mode bits are input to 2 I/O pins for total 8 cycles, followed by dummy cycles. The 4 upper address bits are ignored. The number of dummy cycles is defined beforehand by the frequency of SCK, and configured by the latency bit of LC1 and LC0. The op-code, the address and the mode bits are latched on the rising edge of SCK. After that, FeRAM memory cell array data are shifted out 2 bits at one time through 2 I/O pins synchronously to the falling edge of SCK. When $\overline{CS}$ is risen, the FRDAD command is completed, otherwise it keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 4 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.

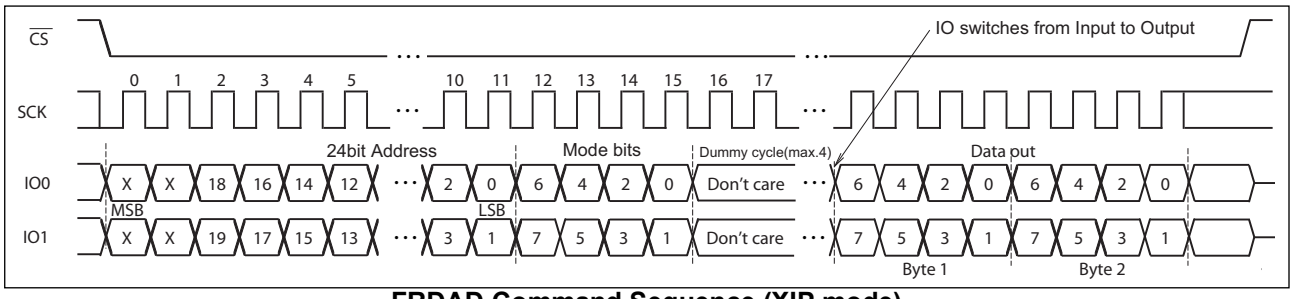
  Address jumps can be done without the need for additional FRDAD command. This is controlled through the setting of the Mode bits after the address sequence. This added feature, which is called “XIP mode”, removes the need for the command sequence. If the Mode bits equal EF_H or AF_H, then the device remains in FRDAD mode and the next address can be entered (after $\overline{CS}$ is raised high and then asserted low) without requiring the FRDAD command, thus eliminating 8 cycles for the command sequence. If the Mode bits are any value other than EF_H and AF_H, then the next time $\overline{CS}$ is raised high the device will be released from FRDAD mode. After that, the device can accept SPI/Dual SPI/Quad SPI commands. $\overline{CS}$ should not be driven high during mode or dummy bits as this may make the mode bits indeterminate.

  It is important that the I/O pins are set to high-impedance prior to the falling edge of the first data out clock. The FRDAD command is terminated by driving $\overline{CS}$ high at any time during data output.

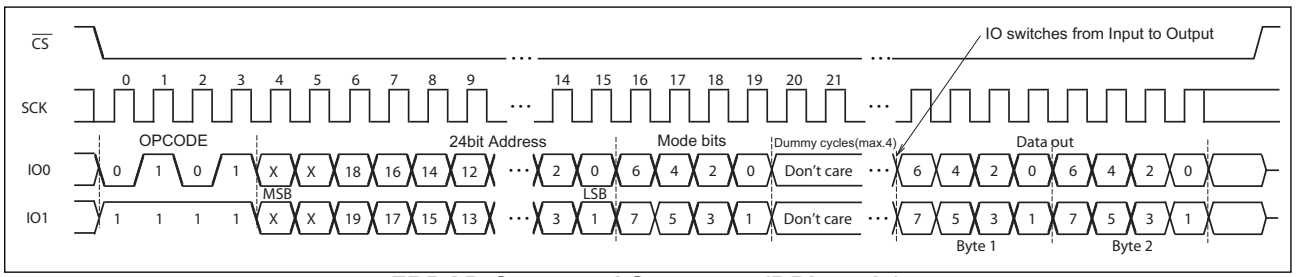
  In DPI Mode, which is set by the EDPI command and is reset by the ESPI, EQPI command, the FRDAD command can be sent 2 bits per SCK rising edge.



FRDAD Command Sequence



FRDAD Command Sequence (XIP mode)

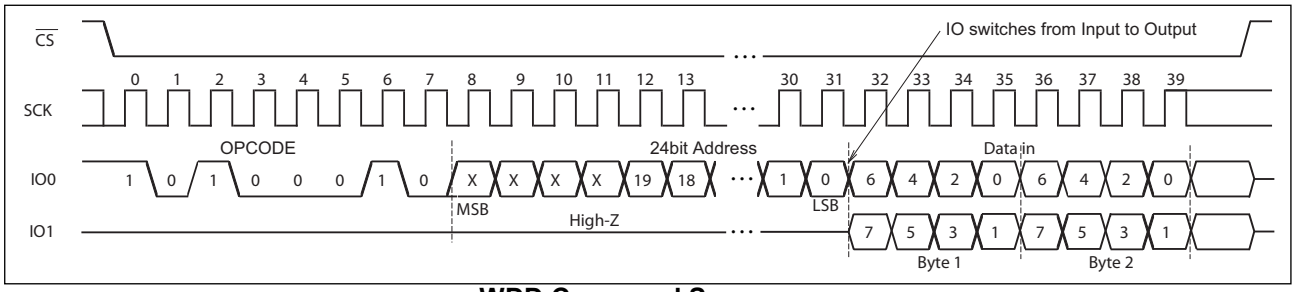


FRDAD Command Sequence (DPI mode)

- **WDD (Write Dual Data)**

  The WDD command is similar to the WRITE command, except that the data is input to 2 I/O pins (IO0 (SI) and, IO1 (SO)) at one time instead of 1 input pin (SI), at a maximum frequency of 108 MHz. The data transfer rate of the WDD command is two times higher than the WRITE command.

  After driving $\overline{CS}$ low, WDD op-code and arbitrary 24 address bits are input to IO0. The 4 upper address bits are ignored. When 8 writing data bits are input to 2 I/O pins for 4 cycles, data is written to FeRAM memory cell array. The op-code, the address and the data are latched on the rising edge of SCK. Risen $\overline{CS}$ will terminate the WDD command. However, if you continue sending the writing data for 8 bits each in unit of 4 cycles before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle keeps on infinitely.



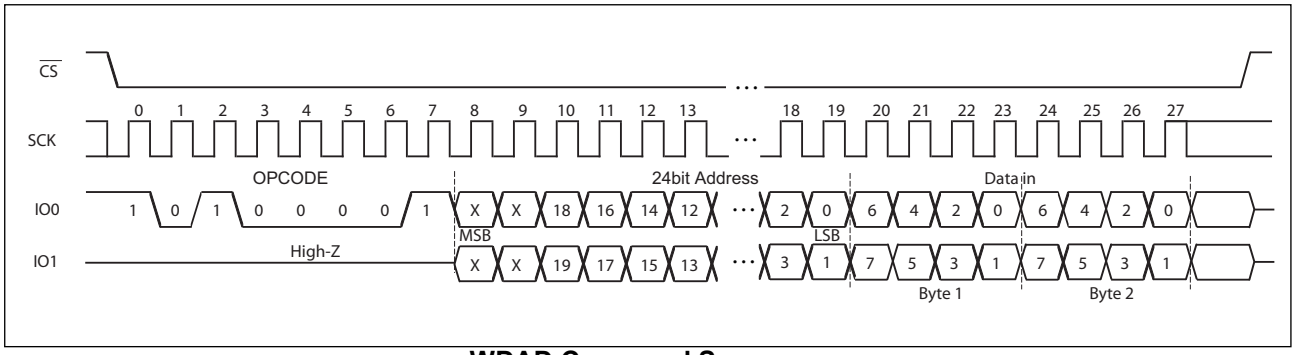
WDD Command Sequence

- **WDAD (Write Dual Address and Data)**

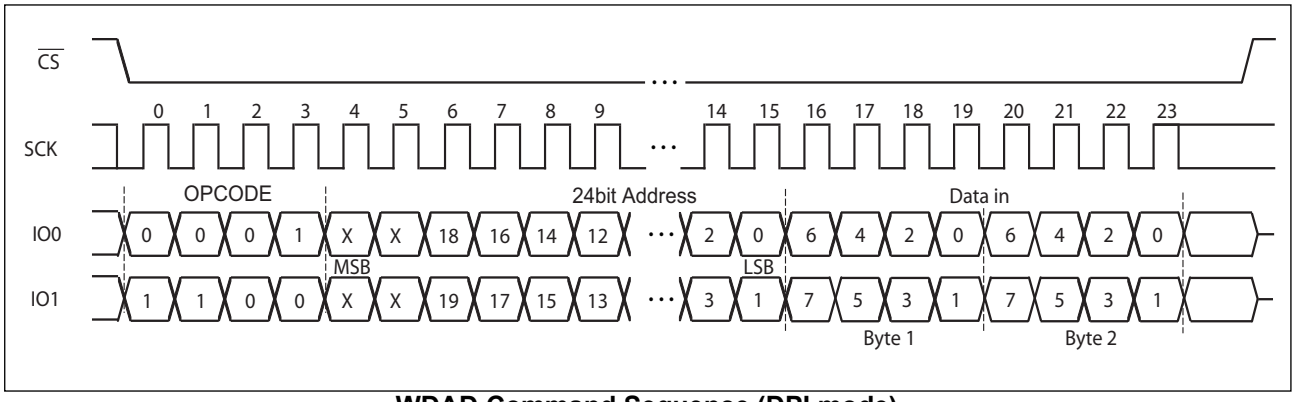
  The WDAD command is similar to the WDD command, except that it further improves throughput by allowing input of the address bits (A23-A0) using 2 bits per SCK via 2 I/O pins (IO0 (SI) and IO1 (SO)), at a maximum frequency of 108 MHz.

  After driving $\overline{CS}$ low, WDAD op-code is input to IO0. Then 24 address bits are input to 2 I/O pins for 12 cycles. The 4 upper address bits are ignored. When 8 writing data bits are input to 2 I/O pins for 4cycles, data is written to FeRAM memory cell array. The opcode, the address and the data are latched on the rising edge of SCK. Risen $\overline{CS}$ will terminate the WDAD command. However, if you continue sending the writing data for 8 bits each in unit of 4 cycles before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle keeps on infinitely.

  In DPI Mode, which is set by the EDPI command and is reset by the ESPI, EQPI command, the WDAD command can be sent 2 bits per SCK rising edge.



WDAD Command Sequence



WDAD Command Sequence (DPI mode)

■ QUAD SPI MODE COMMAND

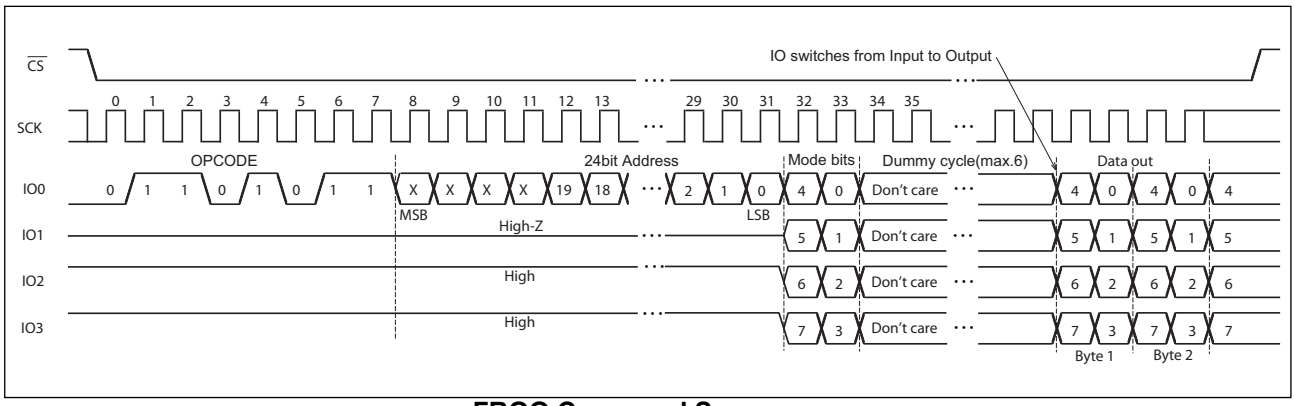
- **FRQO (Fast Read Quad Output)**

The FRQO command is similar to the FSTRD command, except that the data is shifted out 4 bits at one time using 4 I/O pins (IO0 (SI), IO1 (SO), IO2 ($\overline{WP}$) and IO3 ($\overline{HOLD}$)) instead of 1 bit, at a maximum frequency of 108 MHz. The data transfer rate of the FRQO command is four times higher than the FSTRD command.

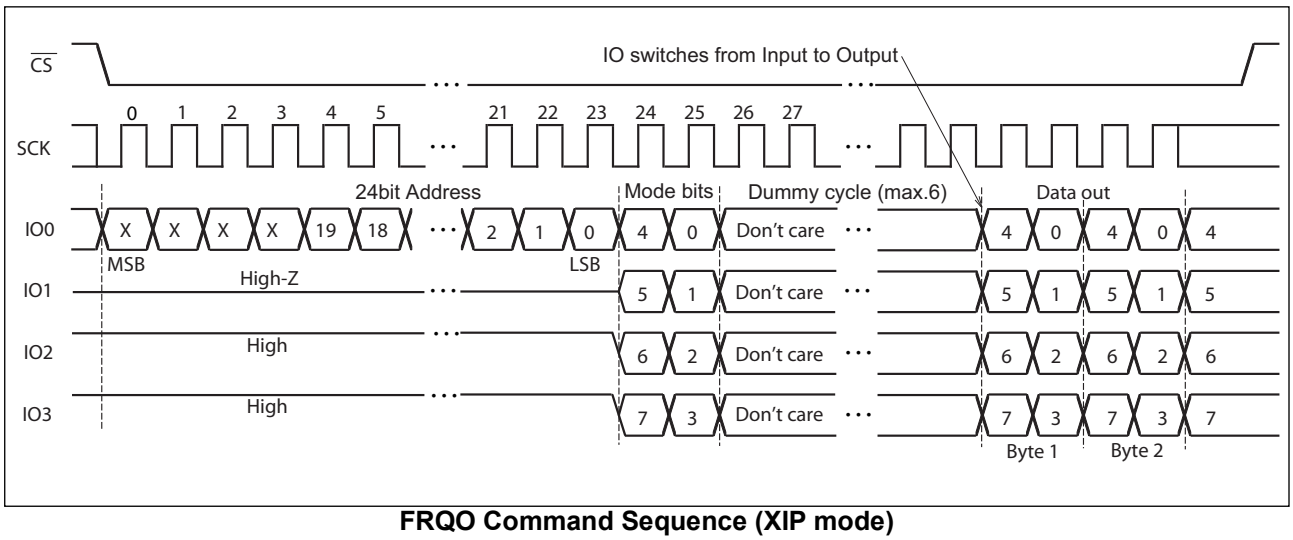
After driving $\overline{CS}$ low, FRQO op-code and arbitrary 24 address bits are input to IO0. The 4 upper address bits are ignored. Then 8 mode bits are input to 4 I/O pins for 2 cycles, followed by dummy cycles. The number of dummy cycles is defined beforehand by the frequency of SCK, and configured by the latency bit of LC1 and LC0. The op-code, the address and the mode bits are latched on the rising edge of SCK. After that, FeRAM memory cell array data are shifted out 4 bits at one time through 4 I/O pins synchronously to the falling edge of SCK. When $\overline{CS}$ is risen, the FRQO command is completed, otherwise it keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 2 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.

Address jumps can be done without the need for additional FRQO command. This is controlled through the setting of the Mode bits after the address sequence. This added feature, which is called “XIP mode”, removes the need for the command sequence. If the Mode bits equal EF_H or AF_H, then the device remains in FRQO mode and the next address can be entered (after $\overline{CS}$ is raised high and then asserted low) without requiring the FRQO command, thus eliminating 8 cycles for the command sequence. If the Mode bits are any value other than EF_H and AF_H, then the next time $\overline{CS}$ is raised high the device will be released from FRQO mode. After that, the device can accept SPI commands. $\overline{CS}$ should not be driven high during mode or dummy bits as this may make the mode bits indeterminate.

It is important that the I/O pins are set to high-impedance prior to the falling edge of the first data out clock. The FRQO command is terminated by driving $\overline{CS}$ high at any time during data output.



FRQO Command Sequence



FRQO Command Sequence (XIP mode)

- **FRQAD (Fast Read Quad Address and Data)**

  The FRQAD command is similar to the FRQO command, except that it further improves throughput by allowing input of the address bits (A23-A0) using 4 bits per SCK via 4 I/O pins (IO0 (SI), IO1 (SO), IO2 ($\overline{WP}$) and IO3 ($\overline{HOLD}$)), at a maximum frequency of 108 MHz.

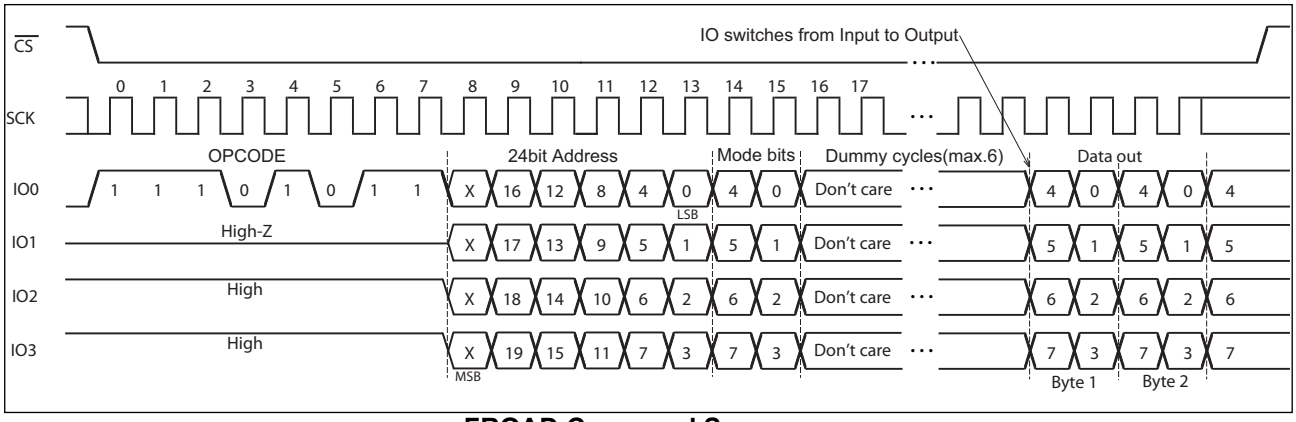
  After driving $\overline{CS}$ low, FRQAD op-code is input to IO0. Then 24 address bits and 8 mode bits are input to 4 I/O pins for total 8 cycles, followed by dummy cycles. The 4 upper address bits are ignored. The number of dummy cycles is defined beforehand by the frequency of SCK, and configured by the latency bit of LC1 and LC0. The op-code, the address and the mode bits are latched on the rising edge of SCK. After that, FeRAM memory cell array data are shifted out 4 bits at one time through 4 I/O pins synchronously to the falling edge of SCK. When $\overline{CS}$ is risen, the FRQAD command is completed, otherwise it keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 2 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.

  FRQAD command cannot be issued soon after power-on. Any other command shall be issued at least once before FRQAD command.

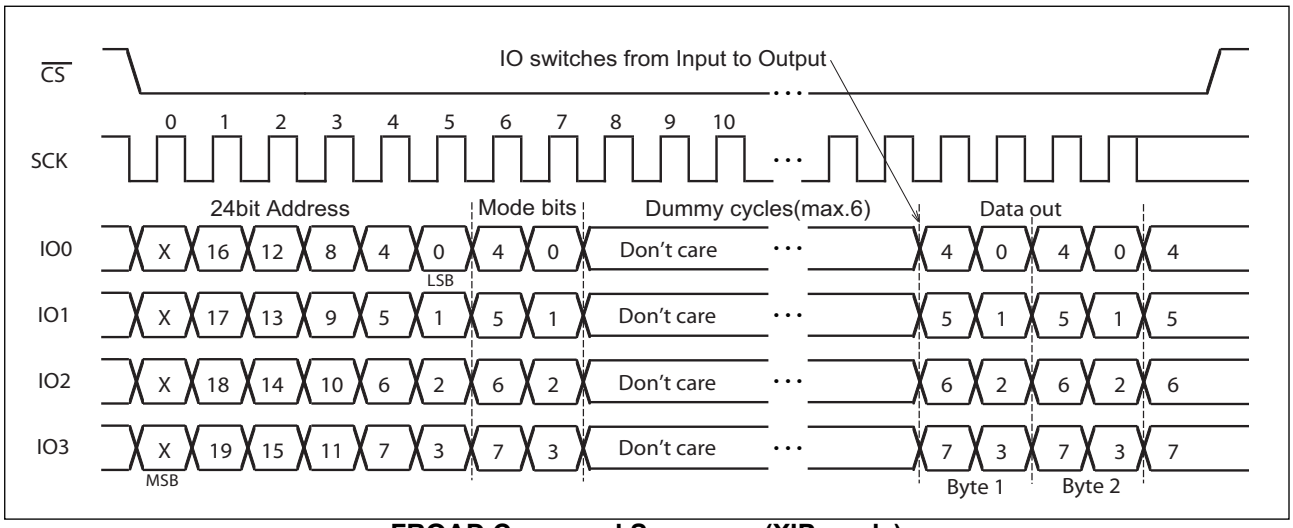
  Address jumps can be done without the need for additional FRQAD command. This is controlled through the setting of the Mode bits after the address sequence. This added feature, which is called “XIP mode”, removes the need for the command sequence. If the Mode bits equal EF_H or AF_H, then the device remains in FRQAD mode and the next address can be entered (after $\overline{CS}$ is raised high and then asserted low) without requiring the FRQAD command, thus eliminating 8 cycles for the command sequence. If the Mode bits are any value other than EF_H and AF_H, then the next time $\overline{CS}$ is raised high the device will be released from FRQAD mode. After that, the device can accept SPI/Dual SPI/Quad SPI commands. $\overline{CS}$ should not be driven high during mode or dummy bits as this may make the mode bits indeterminate.

  It is important that the I/O pins are set to high-impedance prior to the falling edge of the first data out clock. The FRQAD command is terminated by driving $\overline{CS}$ high at any time during data output.

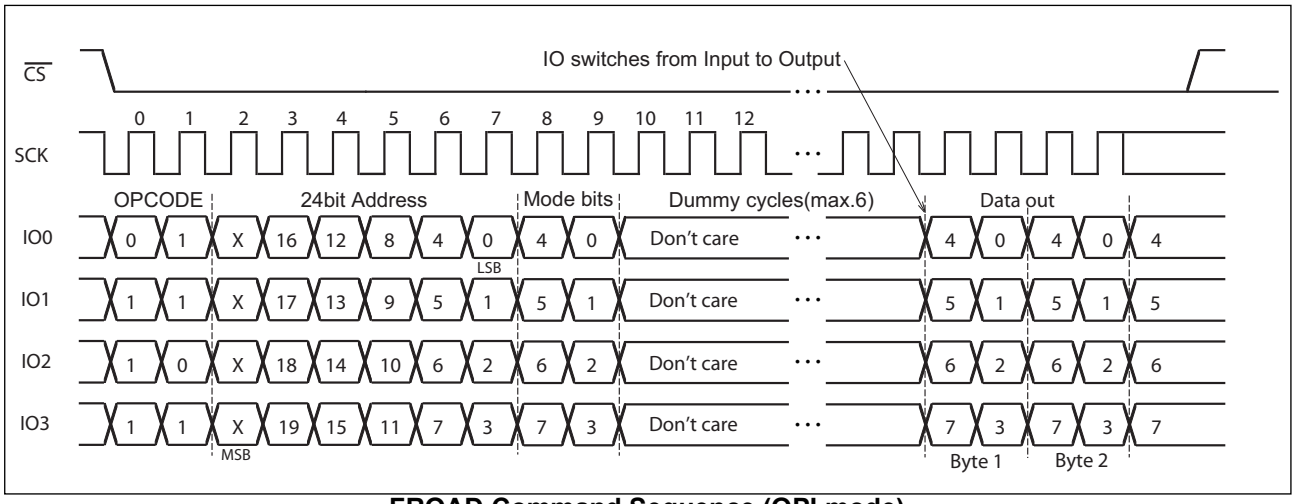
  In QPI Mode, which is set by the EQPI command and is reset by the ESPI, EQPI command, the FRQAD command can be sent 4 bits per SCK rising edge.



FRQAD Command Sequence



FRQAD Command Sequence (XIP mode)

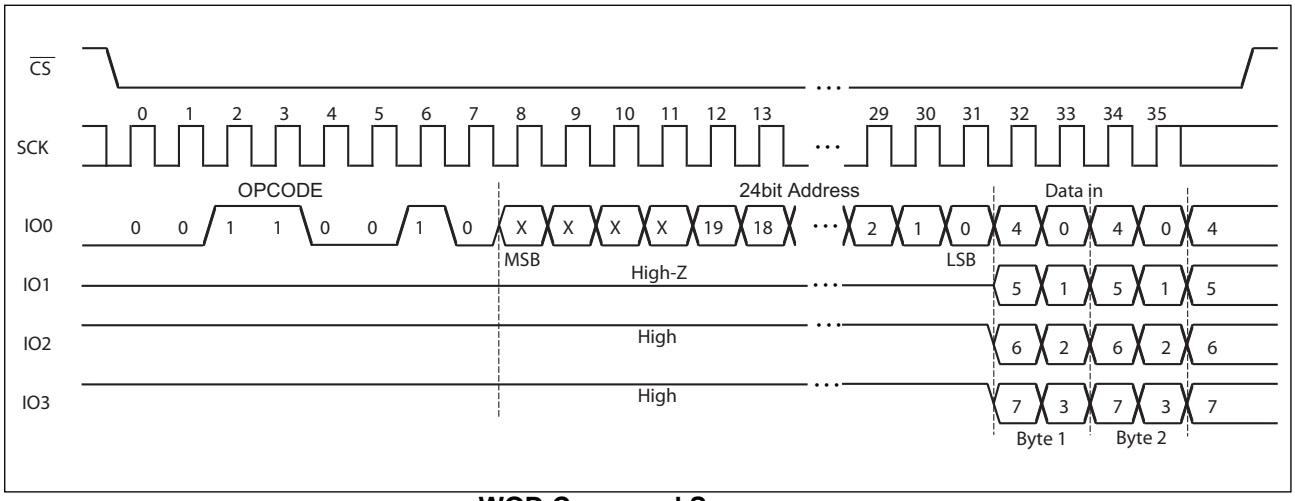


FRQAD Command Sequence (QPI mode)

- **WQD (Write Quad Data)**

  The WQD command is similar to the WRITE command, except that the data is input to 4 I/O pins (IO0 (SI), IO1 (SO), IO2 ($\overline{WP}$) and IO3 ($\overline{HOLD}$)) at one time instead of 1 input pin (SI), at a maximum frequency of 108 MHz. The data transfer rate of the WQD command is four times higher than the WRITE command.

  After driving $\overline{CS}$ low, WQD op-code and arbitrary 24 address bits are input to IO0. The 4 upper address bits are ignored. When 8 writing data bits are input to 4 I/O pins for 2 cycles, data is written to FeRAM memory cell array. The op-code, the address and the data are latched on the rising edge of SCK. Risen $\overline{CS}$ will terminate the WQD command. However, if you continue sending the writing data for 8 bits each in unit of 2 cycles before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle keeps on infinitely.



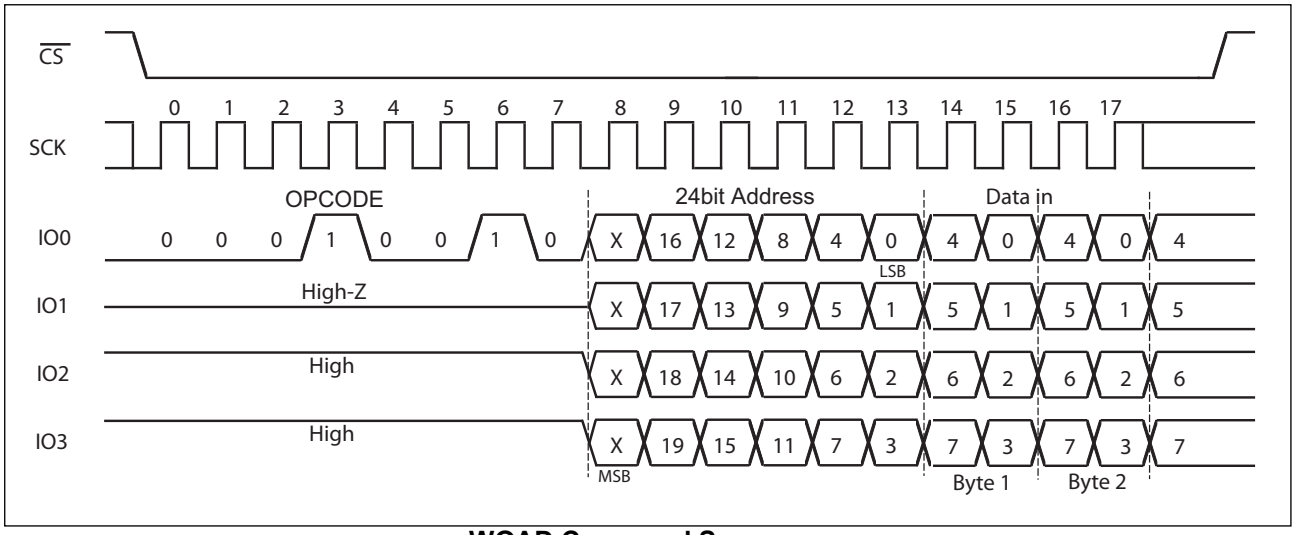
WQD Command Sequence

- **WQAD (Write Quad Address and Data)**

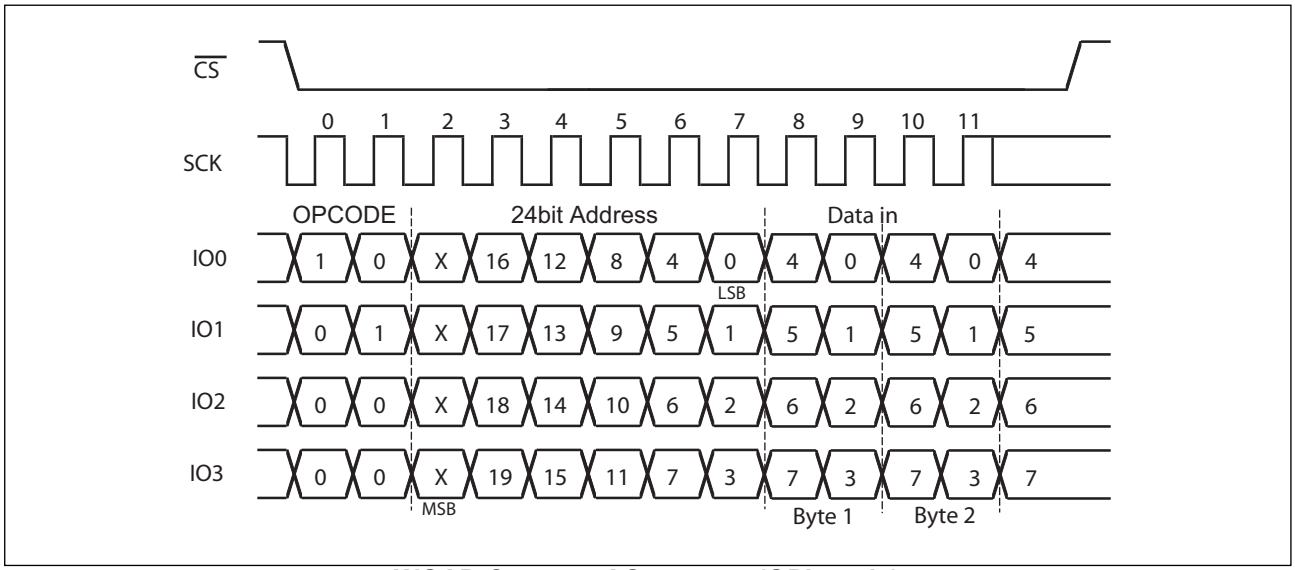
The WQAD command is similar to the WQD command, except that it further improves throughput by allowing input of the address bits (A23-A0) using 4 bits per SCK via 4 I/O pins (IO0 (SI), IO1 (SO), IO2 ($\overline{WP}$) and IO3 ($\overline{HOLD}$)), at a maximum frequency of 108 MHz.

After driving $\overline{CS}$ low, WQAD op-code is input to IO0. Then 24 address bits are input to 4 I/O pins for 6 cycles. The 4 upper address bits are ignored. When 8 writing data bits are input to 4 I/O pins for 2cycles, data is written to FeRAM memory cell array. The opcode, the address and the data are latched on the rising edge of SCK. Risen $\overline{CS}$ will terminate the WQAD command. However, if you continue sending the writing data for 8 bits each in unit of 2 cycles before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle keeps on infinitely.

In QPI Mode, which is set by the EQPI command and is reset by the ESPI, EDPI command, the WQAD command can be sent 4 bits per SCK rising edge.



WQAD Command Sequence



WQAD Command Sequence (QPI mode)

■ DPI MODE COMMAND

DPI Mode can shorten op-code input cycle from 8 cycles to 4 cycles with 2 I/O pins. The device enters DPI Mode with the EDPI Command. When in DPI Mode, the Status Register2 bit5 is set to “1”. the status register2 bit5 will reset to “0” either when the device exits from the DPI Mode with the ESPI, EQPI command or at power-off. After power-on, QPI mode is disabled.

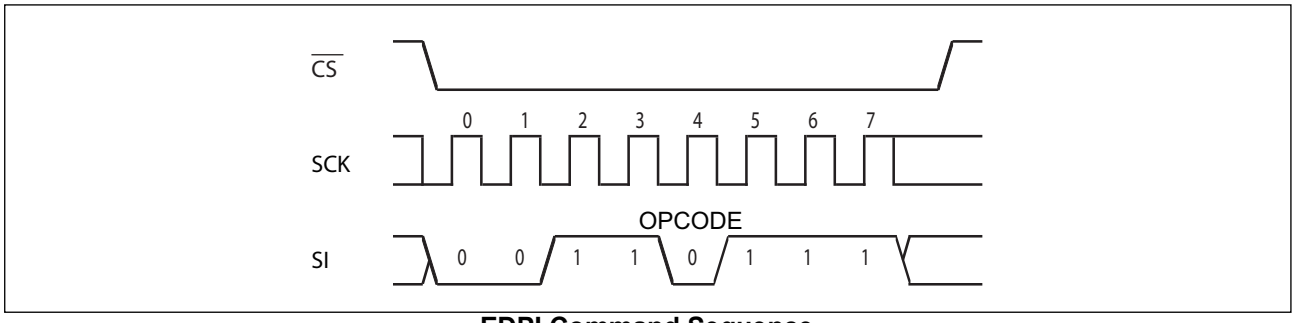
The command list supported in DPI mode

Mode	Name	Description	Op-code	Max Freq. (MHz)	DPI	XIP
SPI	WREN	Set Write Enable Latch	0000 0110B	108	Yes	No
	WRDI	Reset Write Enable Latch	0000 0100B	108	Yes	No
	RDSR	Read Status Register1	0000 0101B	108	Yes	No
	WRSR	Write Status Register1	0000 0001B	108	Yes	No
	RDSR2	Read Status Register2	0011 0101B	108	Yes	No
	WRITE	Write Memory	0000 0010B	108	Yes	No
	RDID	Read Device ID	1001 1111B	108	Yes	No
Dual SPI	FRDO	Fast Read Dual Output	0011 1011B	108*	Yes	Yes
	FRDAD	Fast Read Dual Address and Data	1011 1011B	108*	Yes	Yes
	WDD	Write Dual Data	1010 0010B	108	Yes	No
	WDAD	Write Dual Address and Data	1010 0001B	108	Yes	No
Mode Switch	EQPI	Enable QPI mode	0011 1000B	108	Yes	No
	ESPI	Disable DPI/QPI mode	1111 1111B	108	Yes	No

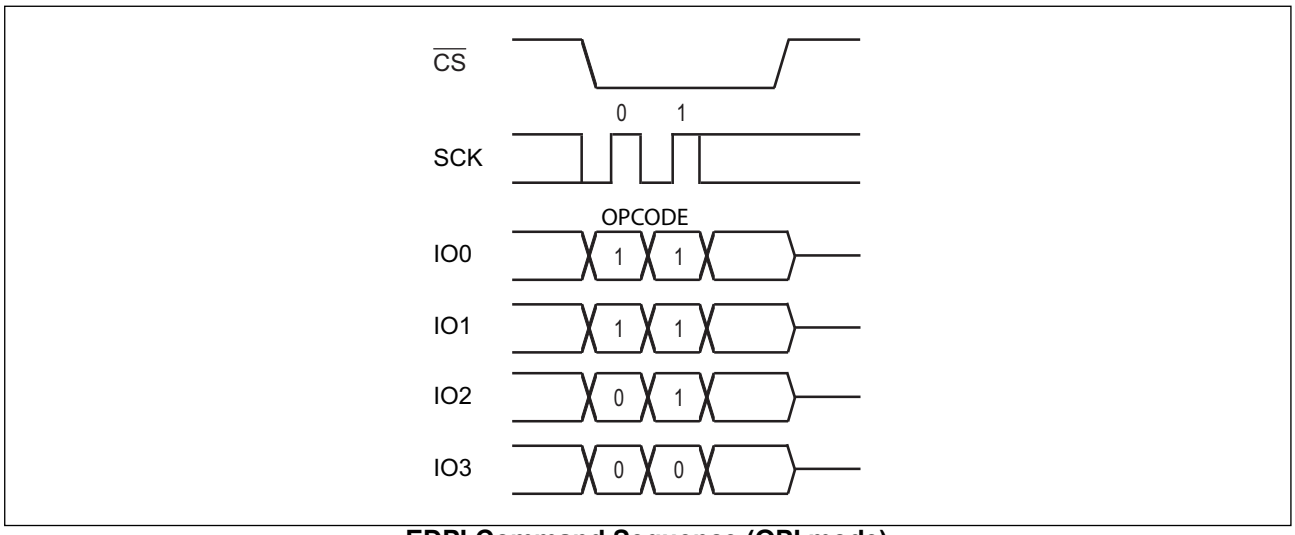
*: The frequency when the number of dummy cycles is maximum value. (see “■ LC MODE”).

- **EDPI (Enable DPI mode)**

The EDPI command is used for the device to enter DPI mode, at a maximum frequency of 108 MHz. After driving $\overline{CS}$ low, the op-code is input to SI(IO0). The command is terminated by driving $\overline{CS}$ high. When in DPI Mode, the Status Register2 bit 5 is set to “1” and the device stays in DPI mode until power-off or the ESPI,EQPI command is issued.



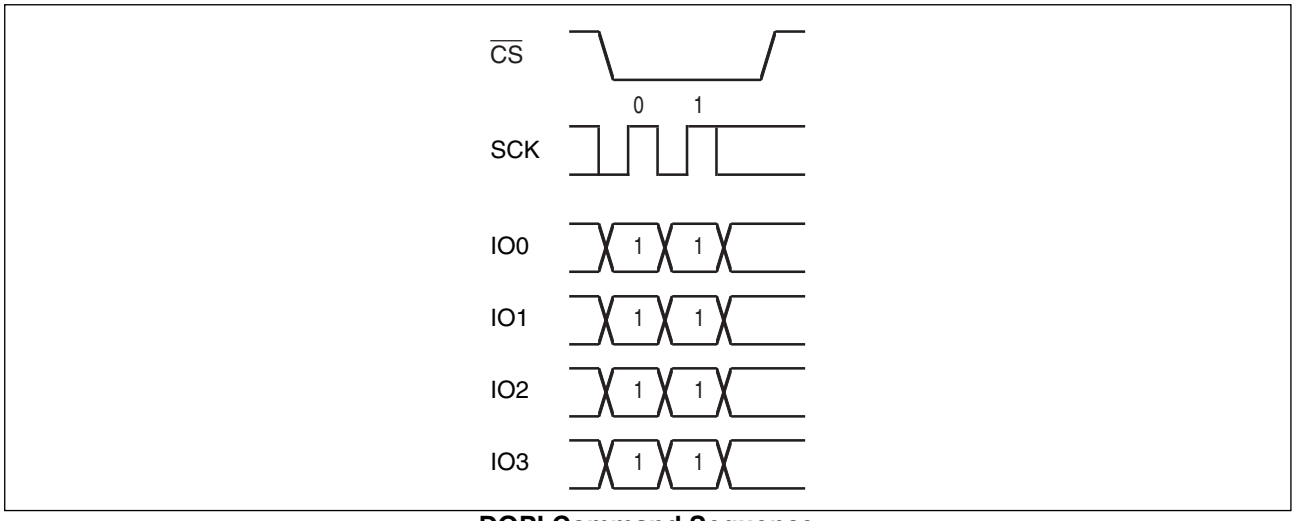
EDPI Command Sequence



EDPI Command Sequence (QPI mode)

- **DQPI (Disable QPI mode)**

  The Disable QPI command is used for the device to exit from QPI mode and return to the SPI mode and set the Status Register bit 6 to “0”, at a maximum frequency of 108 MHz.
  After driving $\overline{CS}$ low, the op-code is input to 4 I/O pins for 2 cycles. The command is terminated by driving $\overline{CS}$ high.



DQPI Command Sequence

■ QPI MODE COMMAND

QPI Mode can shorten op-code input cycle from 8 cycles to 2 cycles with 4 I/O pins. The device enters QPI Mode with the EQPI Command. When in QPI Mode, the Status Register bit 6 is set to “1” and will reset to “0” either when the device exits from the QPI Mode with the SPI, EDPI command or at power-on. After power-on, QPI mode is disabled.

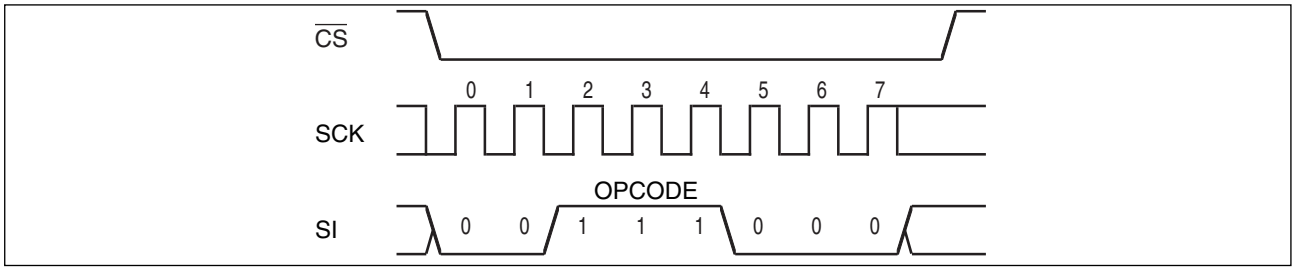
The command list supported in QPI mode

Mode	Name	Description	Op-code	Max Freq. (MHz)	QPI	XIP
SPI	WREN	Set Write Enable Latch	0000 0110B	108	Yes	No
	WRDI	Reset Write Enable Latch	0000 0100B	108	Yes	No
	RDSR	Read Status Register1	0000 0101B	108	Yes	No
	WRSR	Write Status Register1	0000 0001B	108	Yes	No
	RDSR2	Read Status Register2	0011 0101B	108	Yes	No
	WRITE	Write Memory	0000 0010B	108	Yes	No
	RDID	Read Device ID	1001 1111B	108	Yes	No
Quad SPI	FRQO	Fast Read Quad Output	0110 1011B	108*	Yes	Yes
	FRQAD	Fast Read Quad Address and Data	1110 1011B	108*	Yes	Yes
	WQD	Write Quad Data	0011 0010B	108	Yes	No
	WQAD	Write Quad Address and Data	0001 0010B	108	Yes	No
Mode Switch	EDPI	Enable DPI mode	0011 0111B	108	Yes	No
	ESPI	Disable DPI/QPI mode	1111 1111B	108	Yes	No

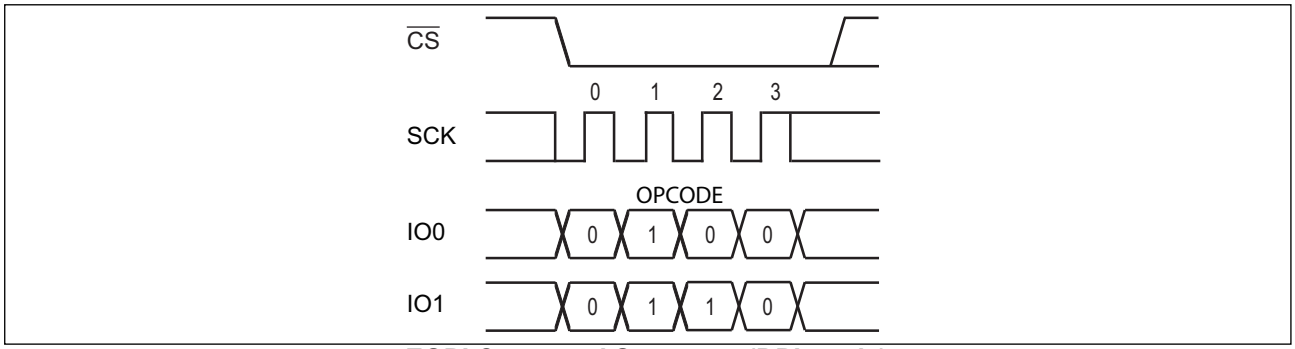
*: The frequency when the number of dummy cycles is maximum value (see “■ LC MODE”).

- **EQPI (Enable QPI mode)**

The EQPI command is used for the device to enter QPI mode, at a maximum frequency of 108 MHz. After driving $\overline{CS}$ low, the op-code is input to SI(IO0). The command is terminated by driving $\overline{CS}$ high. When in QPI Mode, the Status Register bit 6 is set to “1” and the device stays in QPI mode until power-off or the ESPI, EDPI command is issued.



EQPI Command Sequence

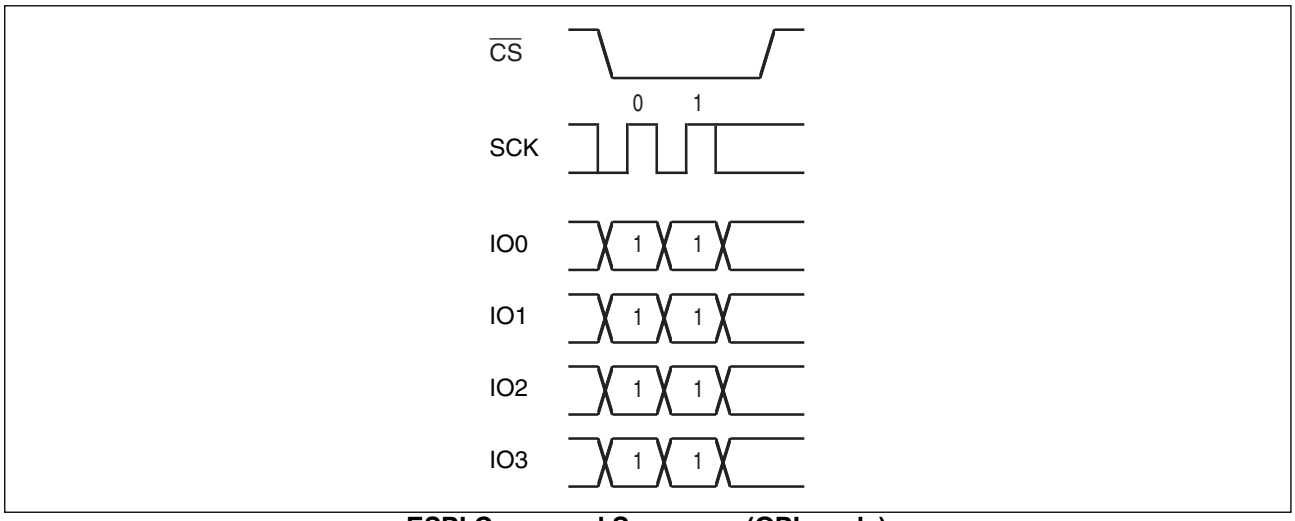


EQPI Command Sequence (DPI mode)

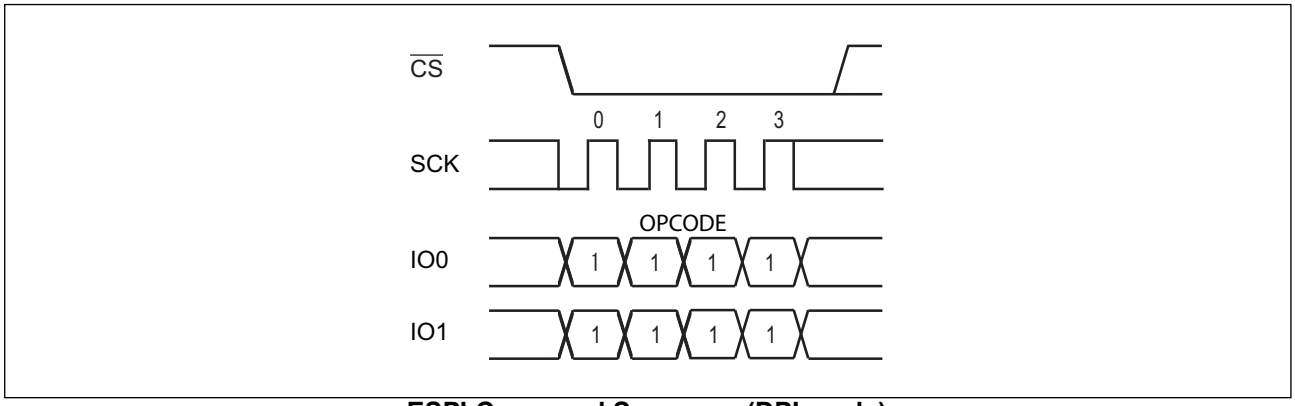
■ Release of DPI/QPI mode

• ESPI (Eable SPI mode)

The ESPI command is used for the device to exit from DPI/QPI mode and return to the SPI mode and set the Status Register2 bit 6/5 to “0”, at a maximum frequency of 108 MHz.
After driving $\overline{CS}$ low, the op-code is input to 4 I/O pins for 2 cycles. The command is terminated by driving $\overline{CS}$ high.



ESPI Command Sequence (QPI mode)



ESPI Command Sequence (DPI mode)

■ BLOCK PROTECT

Writing protect block for WRITE, WDD, WDAD, WQD and WQAD commands are configured by the value of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	C0000H to FFFFFH (upper 1/4)
1	0	80000H to FFFFFH (upper 1/2)
1	1	00000H to FFFFFH (all)

■ WRITING PROTECT

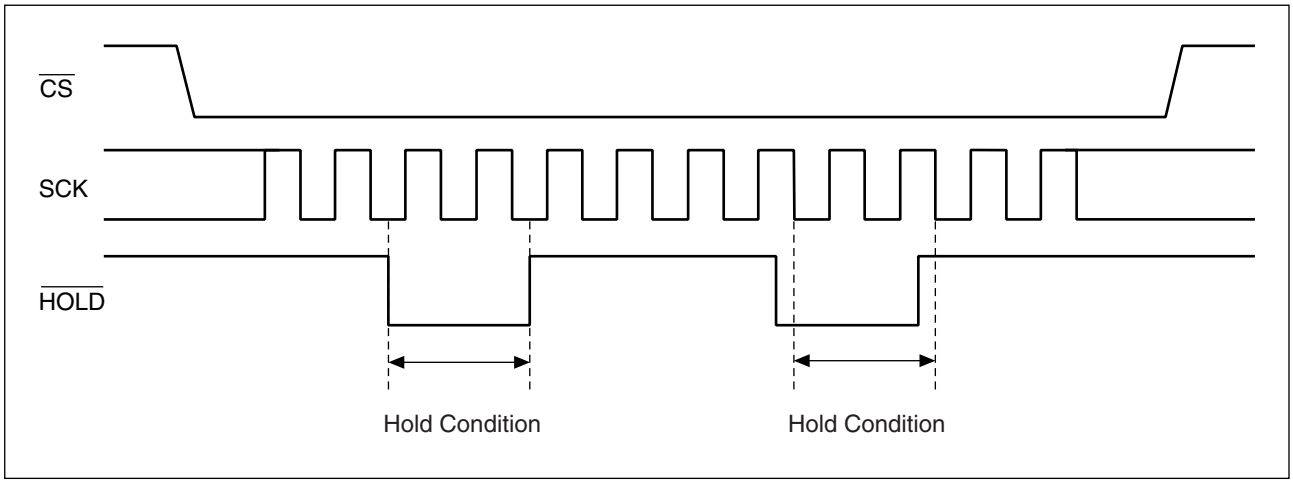
Writing operation of WRITE, WDD, WDAD,WQD, WQAD and the WRSR commands are protected with the value of WEL, WPEN, $\overline{WP}$ as shown in the table.

WEL	WPEN	$\overline{WP}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

■ HOLD OPERATION

Hold status is retained without aborting a command if $\overline{HOLD}$ is “L” level while $\overline{CS}$ is “L” level. The timing for starting and ending hold status depends on the SCK to be “H” level or “L” level when a $\overline{HOLD}$ pin input is transited to the hold condition as shown in the diagram below. In case the $\overline{HOLD}$ pin transited to “L” level when SCK is “L” level, return the $\overline{HOLD}$ pin to “H” level at SCK being “L” level. In the same manner, in case the $\overline{HOLD}$ pin transited to “L” level when SCK is “H” level, return the $\overline{HOLD}$ pin to “H” level at SCK being “H” level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, RDSR2, READ, FSTRD, FRDO, FRDAD). If $\overline{CS}$ is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.

Note: The HOLD operation is disabled during Quad SPI Mode (FRQO, FRQAD, WQD, WQAD) and QPI mode.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 2.5	V
Input voltage*	V_{IN}	− 0.5	V_{DD} + 0.5	V
Output voltage*	V_{OUT}	− 0.5	V_{DD} + 0.5	V
Operation ambient temperature	T_A	− 40	+ 105	°C
Storage temperature	Tstg	− 55	+ 125	°C

*:These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*1	V_{DD}	1.7	1.8	1.95	V
Operation ambient temperature*2	T_A	− 40	—	+ 105	°C

*1: These parameters are based on the condition that V_{SS} is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current	$\|I_{LI}\|$	$\overline{CS}$ = V_{DD}	—	—	1	µA
		$\overline{WP}$, $\overline{HOLD}$, SCK, SI = 0 V to V_{DD}	—	—	1	
Output leakage current	$\|I_{LO}\|$	SO = 0 V to V_{DD}	—	—	1	µA
Operating power supply current	I_{DD}	SCK = 20 MHz (SPI)	—	1.4	—	mA
		SCK = 40 MHz (SPI)	—	2.8	—	mA
		SCK = 108 MHz (SPI)	—	7.5	9	mA
		SCK = 20 MHz (Quad SPI)	—	2.7	—	mA
		SCK = 40 MHz (Quad SPI)	—	5.4	—	mA
		SCK = 108 MHz (Quad SPI)	—	15	18	mA
Standby current	I_{SB}	SCK = SI = $\overline{CS}$ = $\overline{WP}$ = $\overline{HOLD}$ = V_{DD}	—	30	180	µA
Input high voltage	V_{IH}	V_{DD} = 1.7 V to 1.95 V	V_{DD} × 0.8	—	V_{DD} + 0.3	V
Input low voltage	V_{IL}	V_{DD} = 1.7 V to 1.95 V	− 0.5	—	V_{DD} × 0.2	V
Output high voltage	V_{OH}	I_{OH} = − 2 mA	V_{DD} − 0.5	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V

2. AC Characteristics

Parameter	Symbol	Condition	Valu		Unit
			Min	Max	
SCK clock frequency	f_{CK}	except READ command*2	0	108*3	MHz
		for READ command	0	40	MHz
Clock high time	t_{CH}	except READ command	4	—	ns
		for READ command	11	—	ns
Clock low time	t_{CL}	except READ command	4	—	ns
		for READ command	11	—	ns
Chip select set up time	t_{CSU}		5	—	ns
Chip select hold time	t_{CSH}		5	—	ns
Output disable time*2	t_{OD}		—	7	ns
Output data valid time*2	t_{ODV}		—	7	ns
Output hold time	t_{OH}		0	—	ns
Deselect time	t_D	After Write cycle (in SPI/DPI mode)	40	—	ns
		After Write cycle (in QPI mode)	80	—	ns
		After Read cycle (in SPI/DPI mode)	40	—	ns
		After Read cycle (in QPI mode) *1	80	—	ns
		After Read cycle (in XIP mode) *1	100	—	ns
Data set up time	t_{SU}		3	—	ns
Data hold time	t_H		4	—	ns
$\overline{\text{HOLD}}$ set up time	t_{HS}		4	—	ns
$\overline{\text{HOLD}}$ hold time	t_{HH}		4	—	ns
$\overline{\text{HOLD}}$ output floating time*2	t_{HZ}		—	7	ns
$\overline{\text{HOLD}}$ output active time*2	t_{LZ}		—	7	ns

*1 : t_D after read cycle normally equals 40ns. But in QPI mode or XIP mode, t_D will be longer (80ns or 100ns) due to internal cycle time unless read operation is terminated by driving $\overline{CS}$ high in the specific address. In case the read operation is terminated either in A1=1 and other address = “don’t care” during QPI mode or in A1=1, A0=1 and other address = “don’t care” during XIP mode, t_D=40ns can be kept.

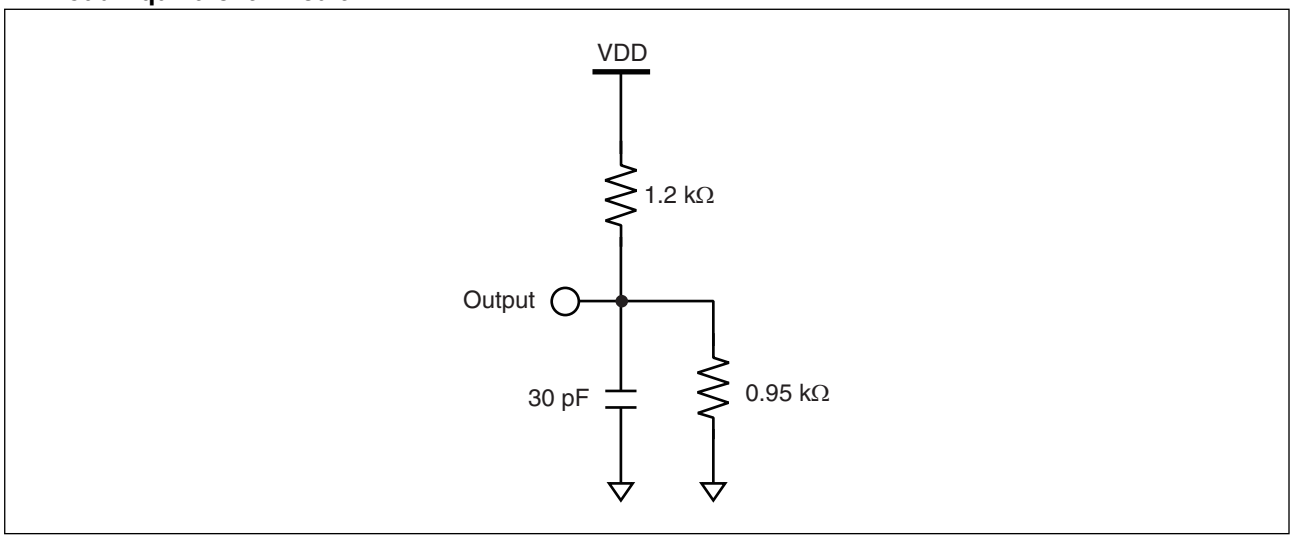
*2 : “AC Load Equivalent Circuit 2” applies to these condition or parameters. Others are tested under “AC Load Equivalent Circuit 1”.

*3 : For the frequency of FRDO, FRDAD, FRQO and FRQAD commands, the number of dummy cycles is maximum value. (see “■ LC MODE”)

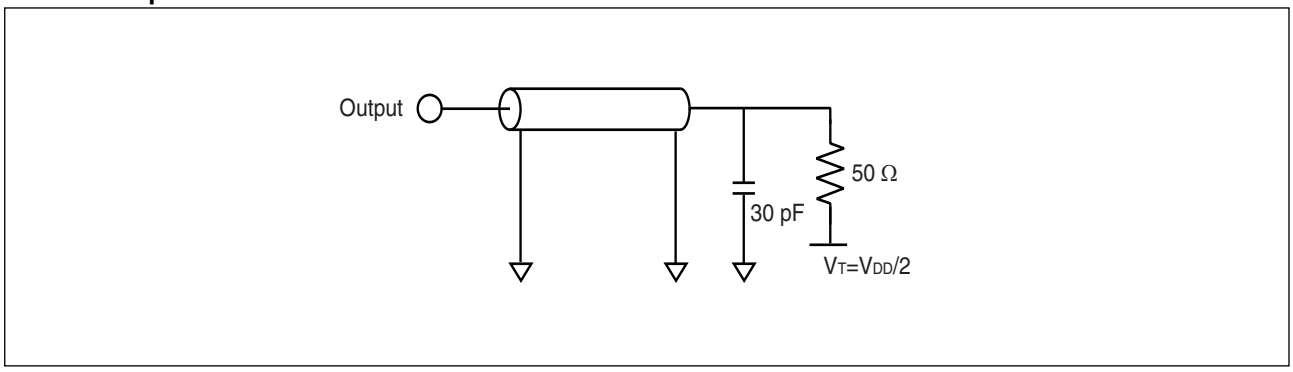
AC Test Condition

Power supply voltage	: 1.7 V to 1.95 V
Operation ambient temperature	: − 40 °C to + 105 °C
Input voltage magnitude	: $V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$
Input rising time	: 2 ns
Input falling time	: 2 ns
Input judge level	: $V_{DD}/2$
Output judge level	: $V_{DD}/2$

AC Load Equivalent Circuit 1



AC Load Equivalent Circuit 2

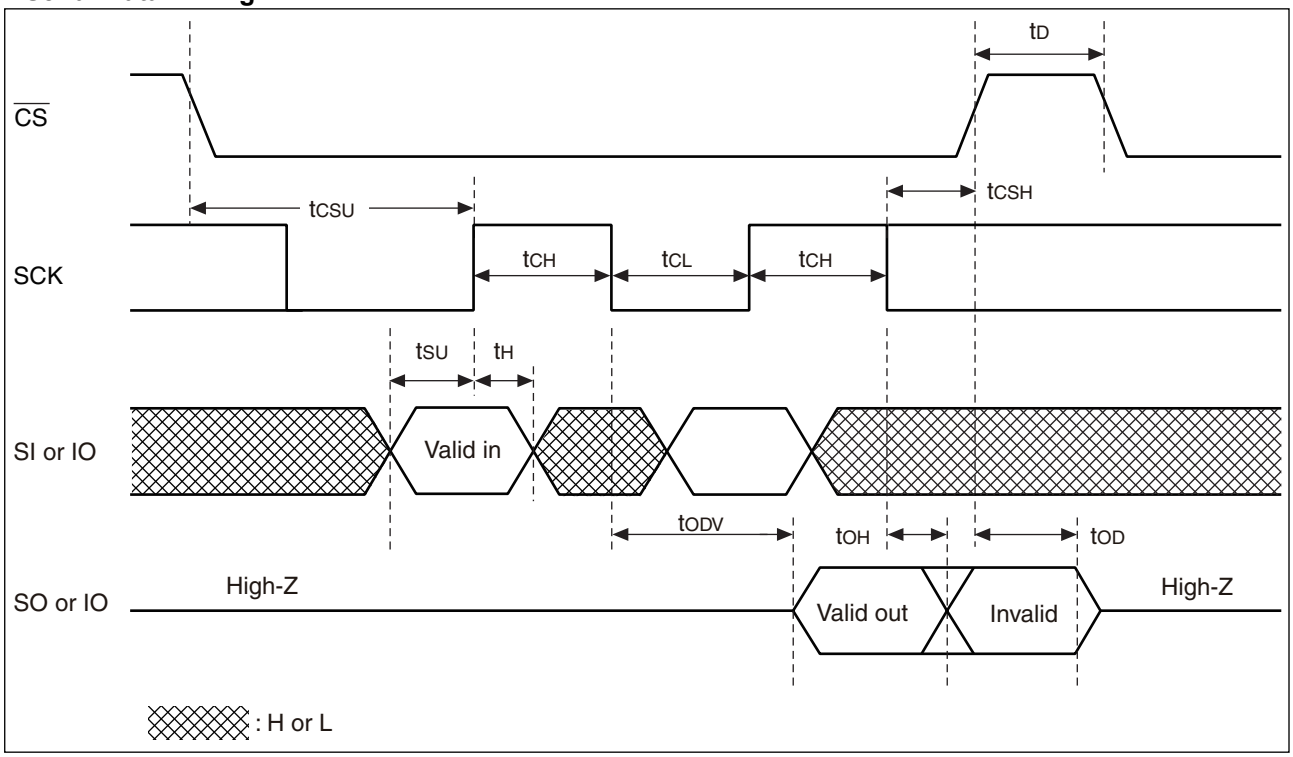


3. Pin Capacitance

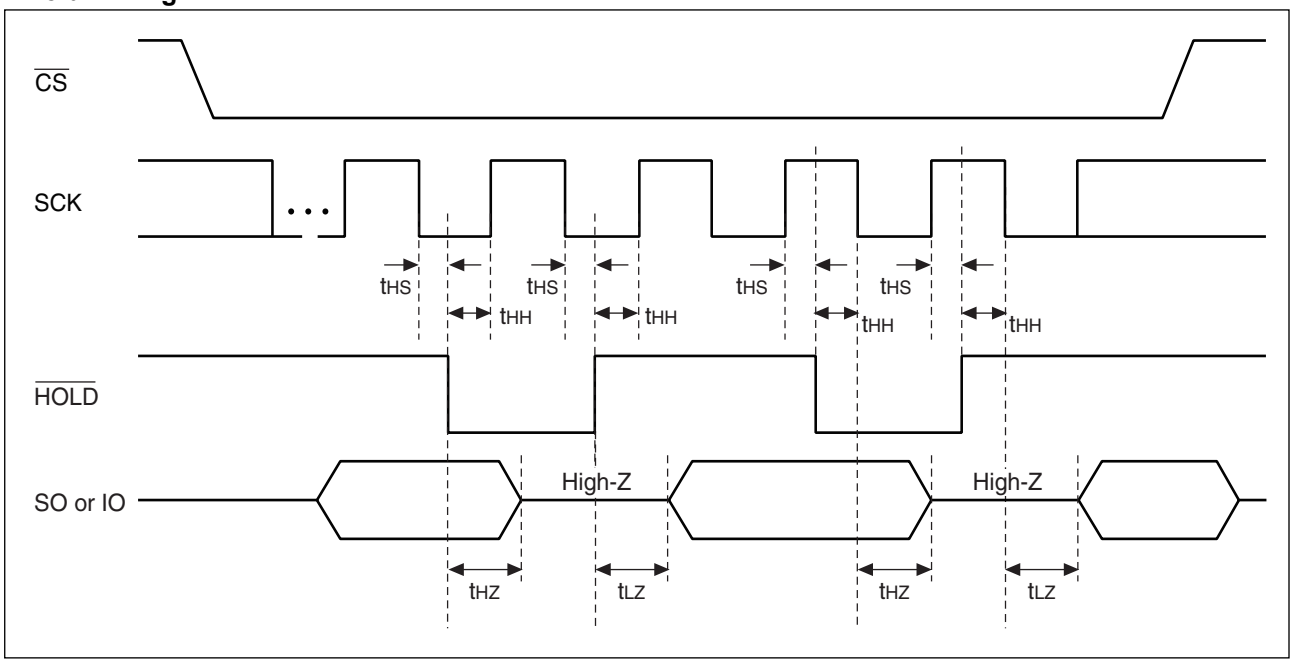
Parameter	Symbol	Condition	Value		Unit
			Min	Max	
I/O capacitance	$C_{I/O}$	$V_{DD} = V_{IN} = V_{OUT} = 0$ V, f = 1 MHz, T_A = +25 °C	—	4	pF
Input capacitance	C_I		—	4	pF

■ TIMING DIAGRAM

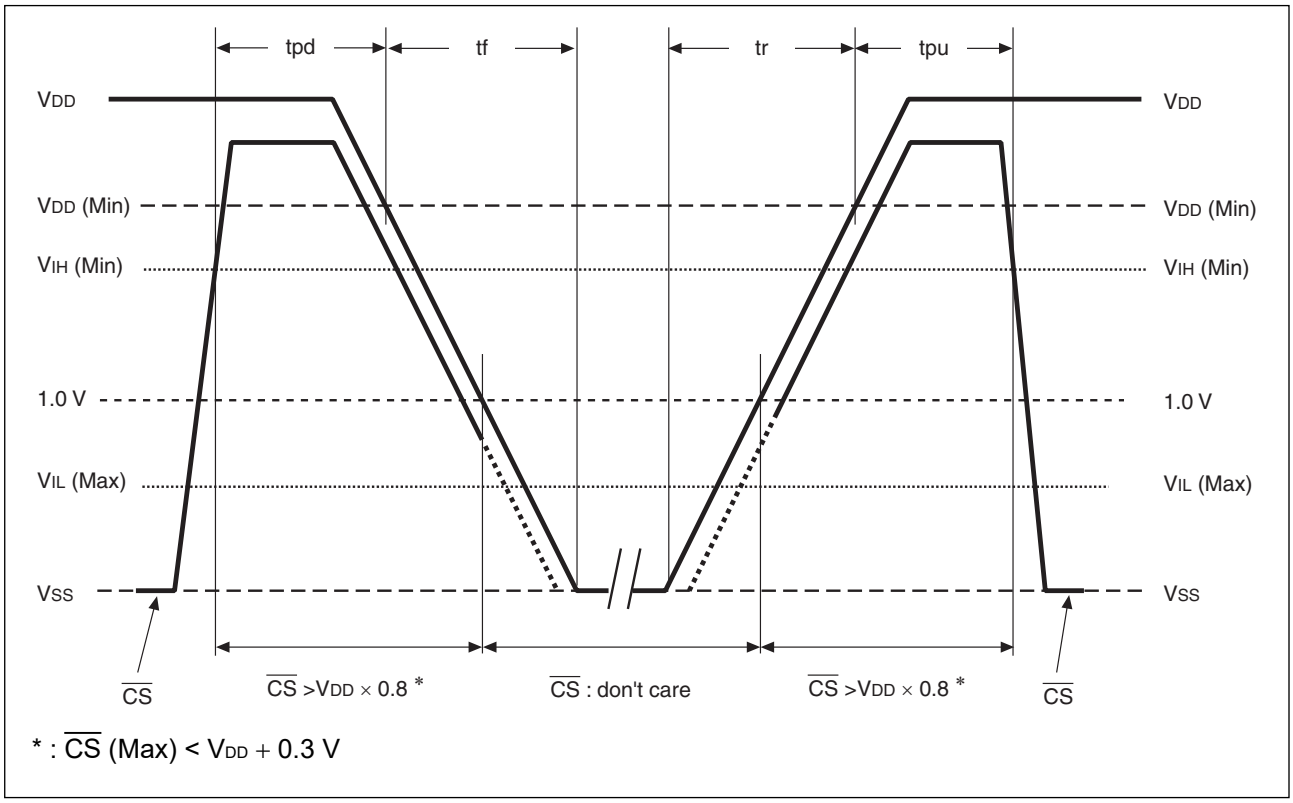
• Serial Data Timing



• Hold Timing



■ POWER ON/OFF SEQUENCE



Parameter	Symbol	Value		Unit
		Min	Max	
$\overline{CS}$ level hold time at power OFF	tpd	400	—	ns
$\overline{CS}$ level hold time at power ON	tpu	250	—	µs
Power supply rising time	tr	0.05	—	ms/V
Power supply falling time	tf	0.1	—	ms/V

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FeRAM CHARACTERISTICS

Parameter	Value		Unit	Remarks
	Min	Max		
Read/Write Endurance*1	10^{13}	—	Times/byte	Operation Ambient Temperature T_A = + 105 °C
Data Retention*2	10	—	Years	Operation Ambient Temperature T_A = + 105 °C
	95	—		Operation Ambient Temperature T_A = + 55 °C
	≥ 200	—		Operation Ambient Temperature T_A = + 35 °C

*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

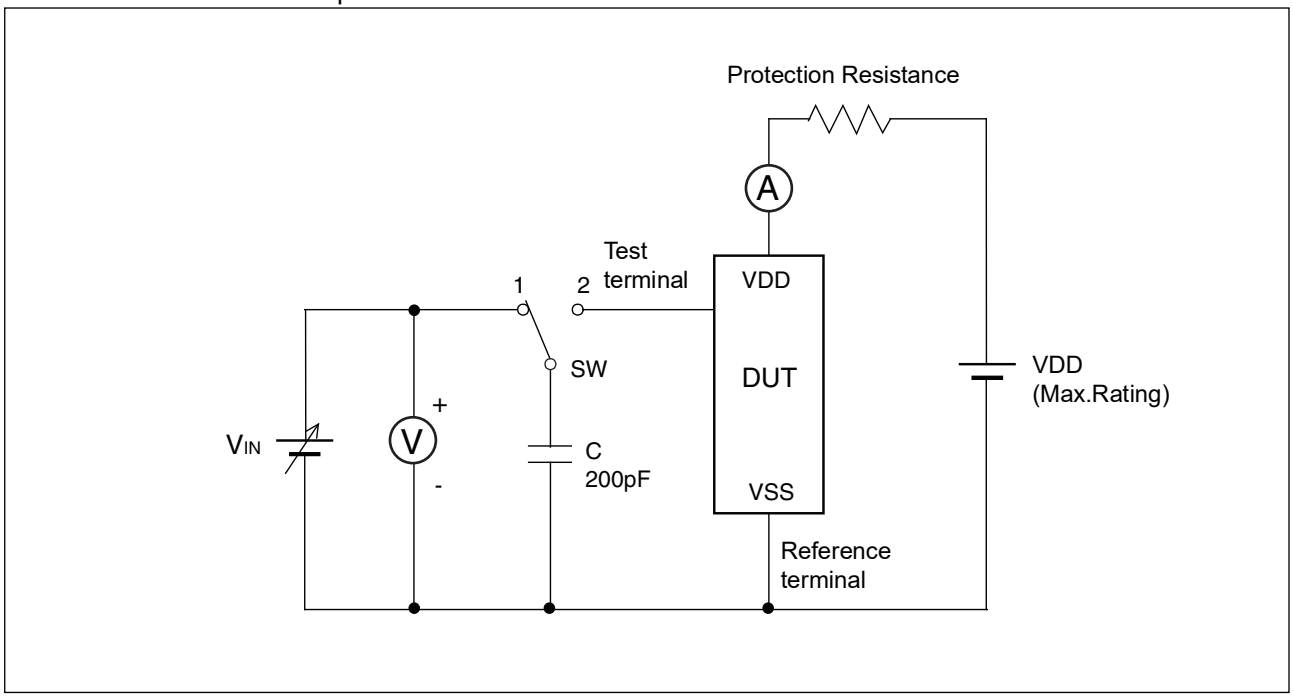
■ NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RQ8MLXPF-G-BCE1 MB85RQ8MLXPF-G-BCERE1	≥ |2000 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		≥ |1000 V|
Latch-Up (C-V Method) Proprietary method		≥ |200 V|

• C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle. Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

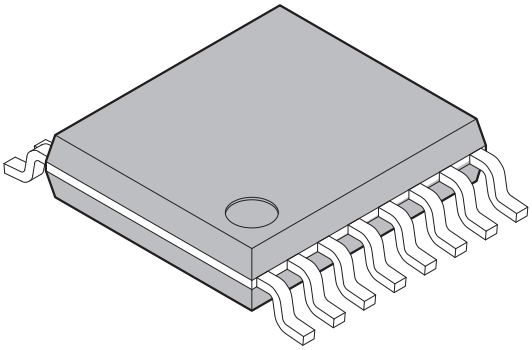
■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RQ8MLXPF-G-BCE1	16-pin plastic SOP	Tray	— *
MB85RQ8MLXPF-G-BCERE1	16-pin plastic SOP	Embossed Carrier tape	500

* : Please contact our sales office about minimum shipping quantity.

■ PACKAGE DIMENSION

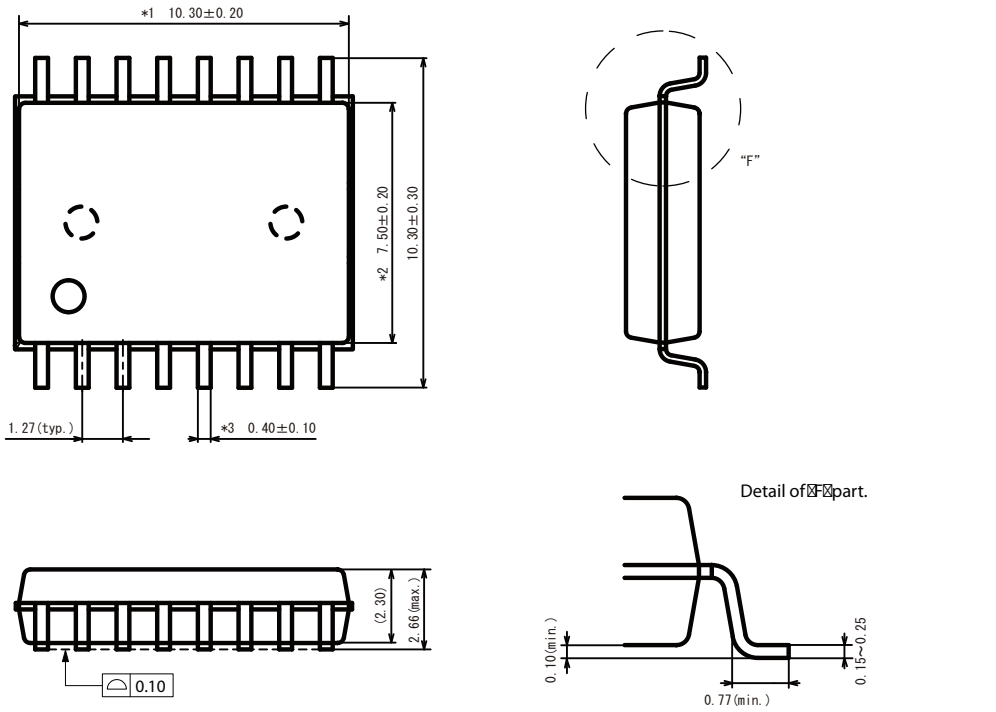
16-pin plastic SOP



Lead pitch	1.27mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	2.66mm MAX

16-pin plastic SOP

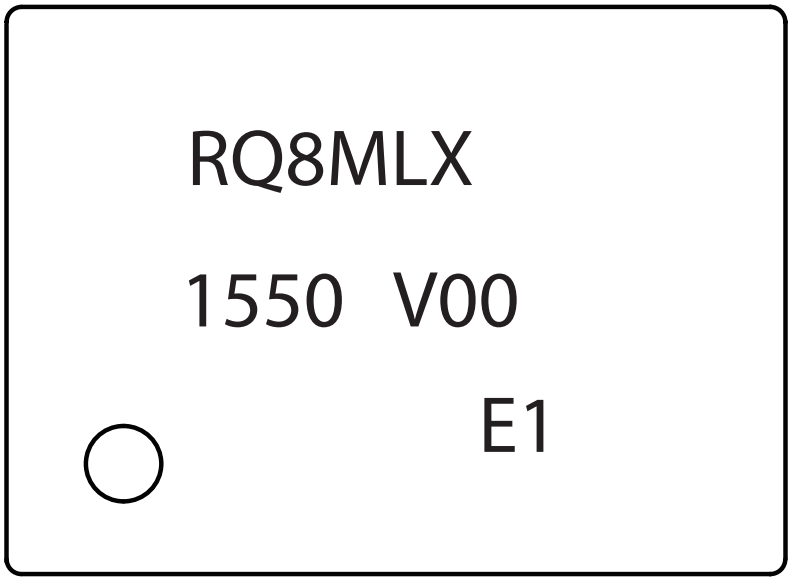
Note 1) *1 does not include Mold flash.
Note 2) *2 does not include Mold flash.
Note 3) *3 does not include TRIM offset.



Dimensions in mm.

■ MARKING

[MB85RQ8MLXPF-G-BCE1]
[MB85RQ8MLXPF-G-BCERE1]



[16-pin plastic SOP]

1500: Year and Week code
V00: Trace code
E1: Environmental code

■ PACKING INFORMATION

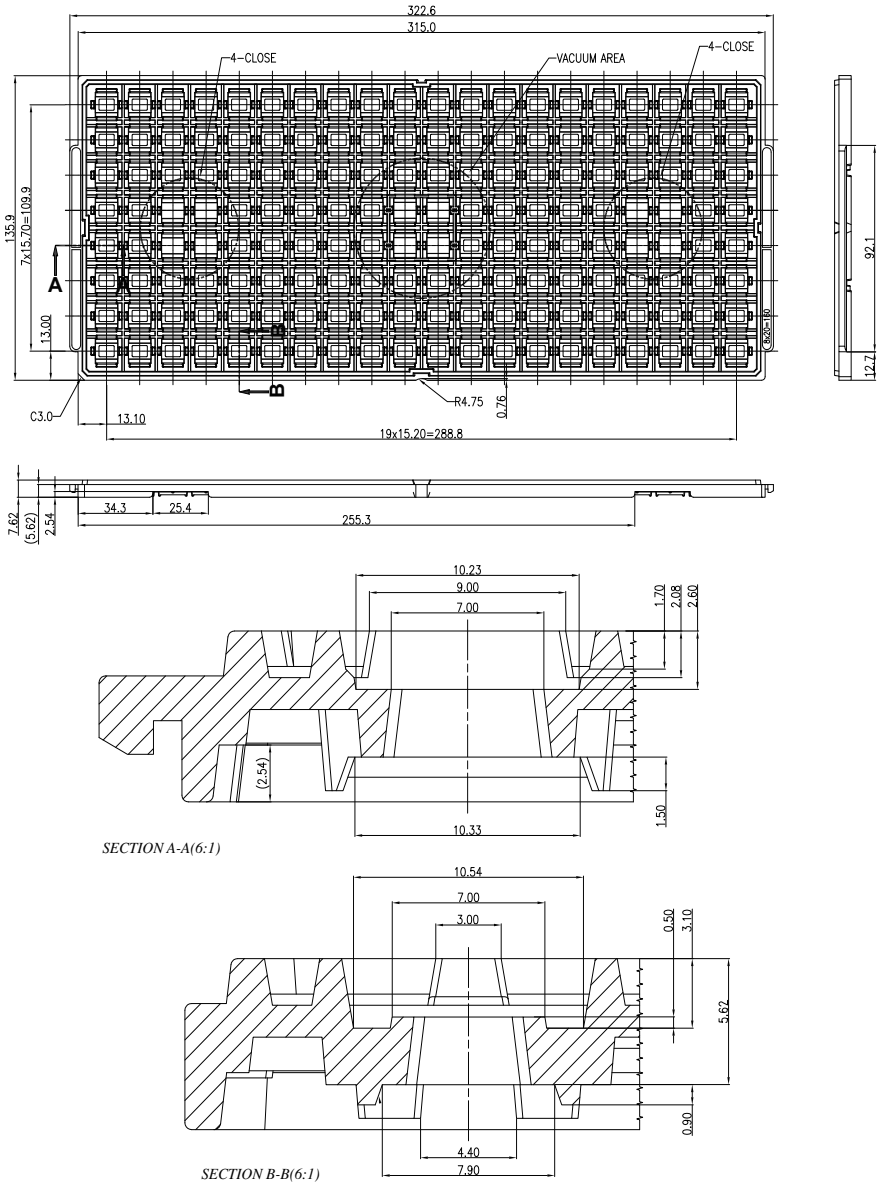
(1) MB85RQ8MLXPF-G-BCE1

1. Tray

1.1 Tray Storage Capacity

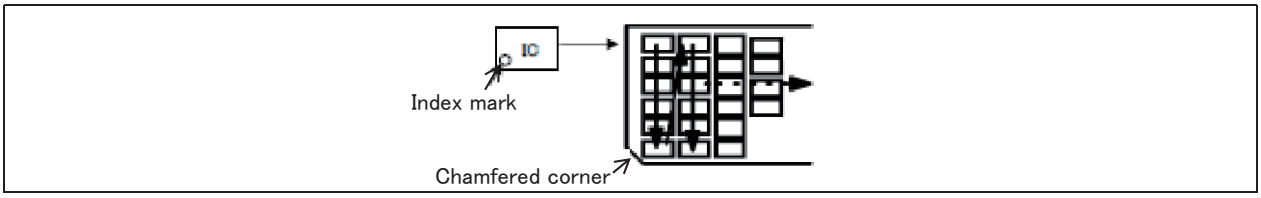
Maximum storage capacity		
pcs/tray	pcs/inner box	pcs/outer box
160	1600	6400

1.2 Tray Dimensions (JEDEC Standard)



(Dimensions in mm)

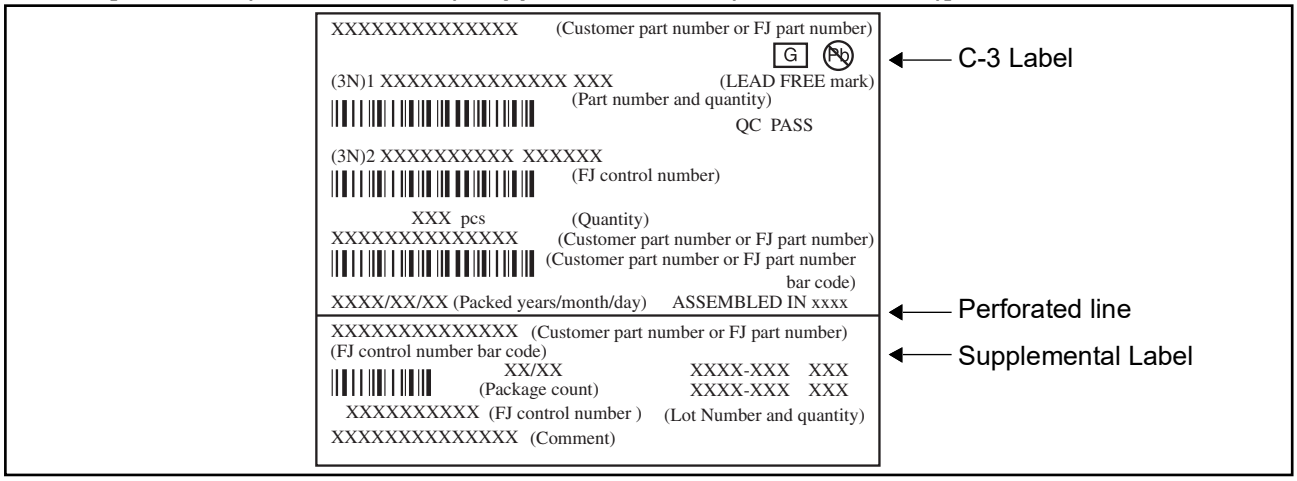
1.3 IC Orientation



1.4 Product label indicators (an example)

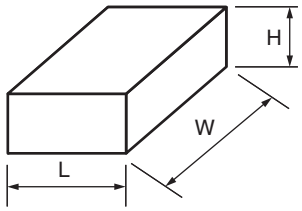
Label on Inner box/Moisture Barrier Bag

[C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



1.5 Dimensions for Containers

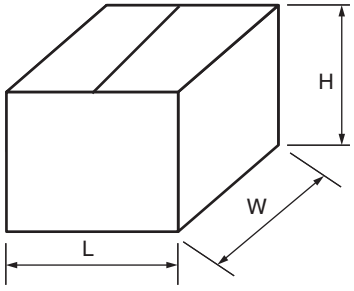
(1) Dimensions for inner box



L	W	H
165	360	75

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
355	385	195

(Dimensions in mm)

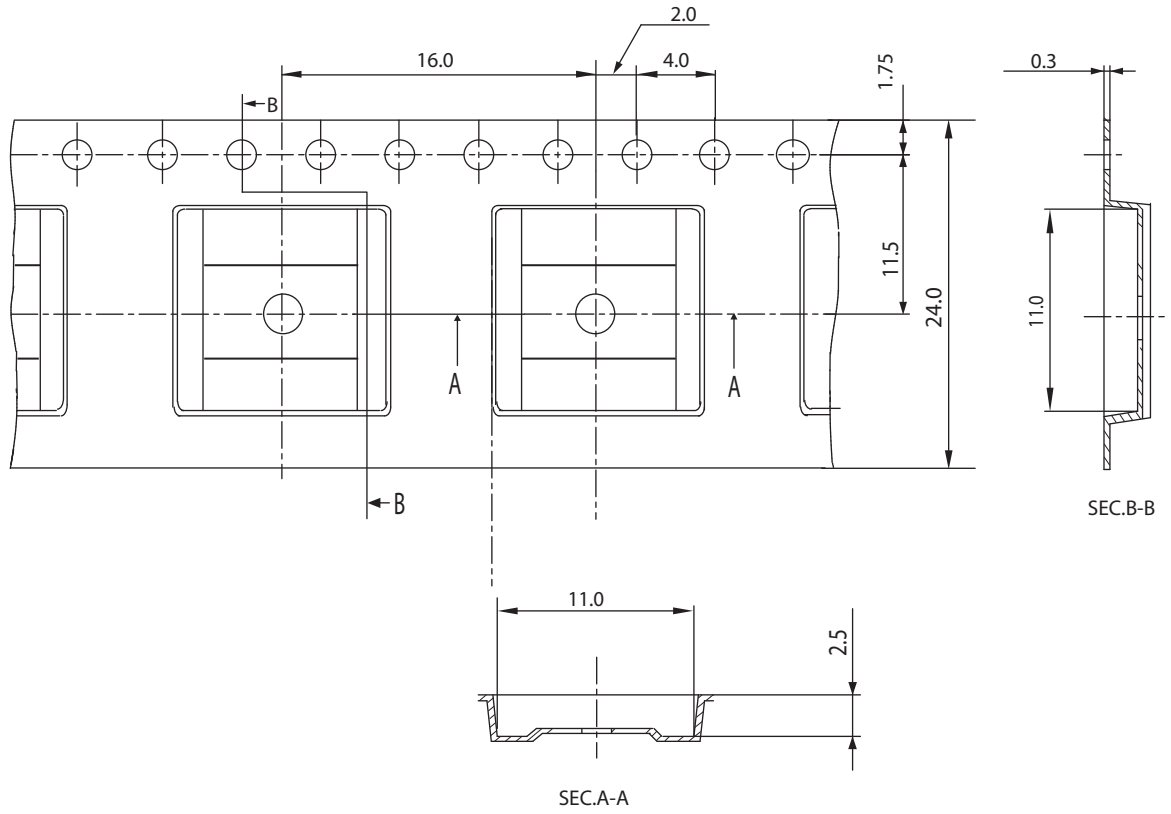
(2) MB85RQ8MLXPF-G-BCERE1

2. Emboss Tape

2.1 IC Storage Capacity

Maximum storage capacity		
pcs/reel	pcs/inner box	pcs/outer box
500	500	3000

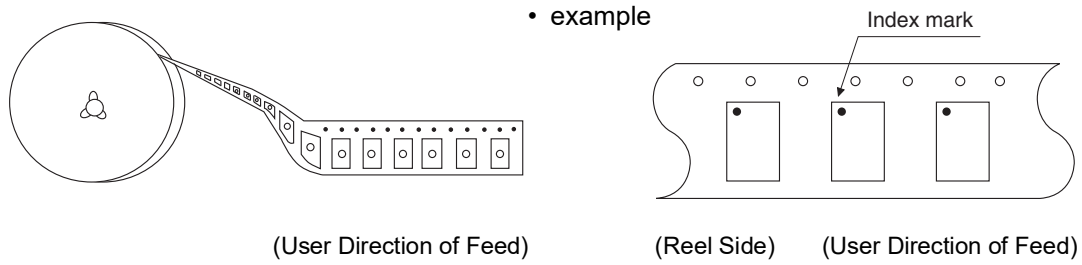
2.2Tape Dimensions



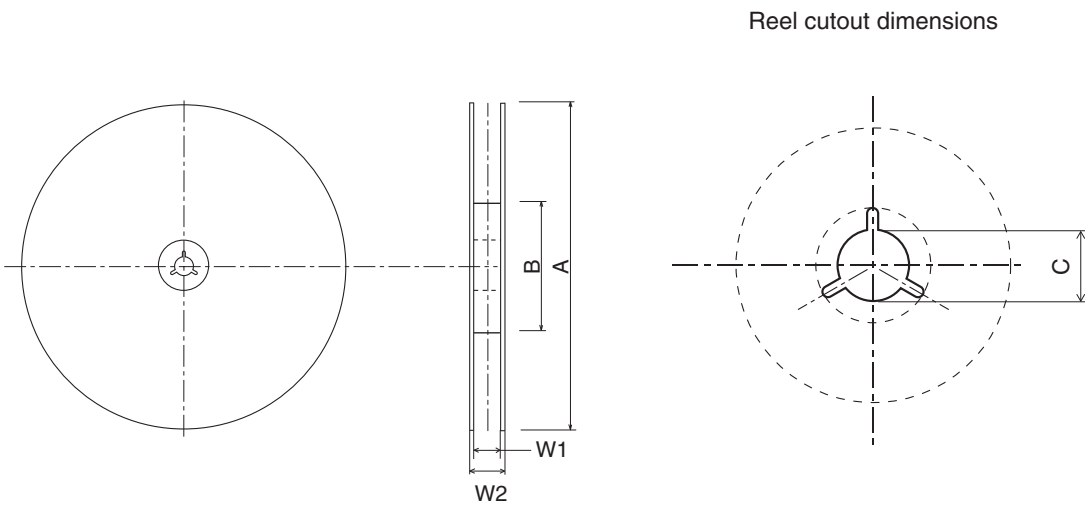
(Dimensions in mm)

Heat proof temperature : No heat resistance.
Package should not be baked by using tape and reel.

2.3 IC orientation



2.4 Reel dimensions

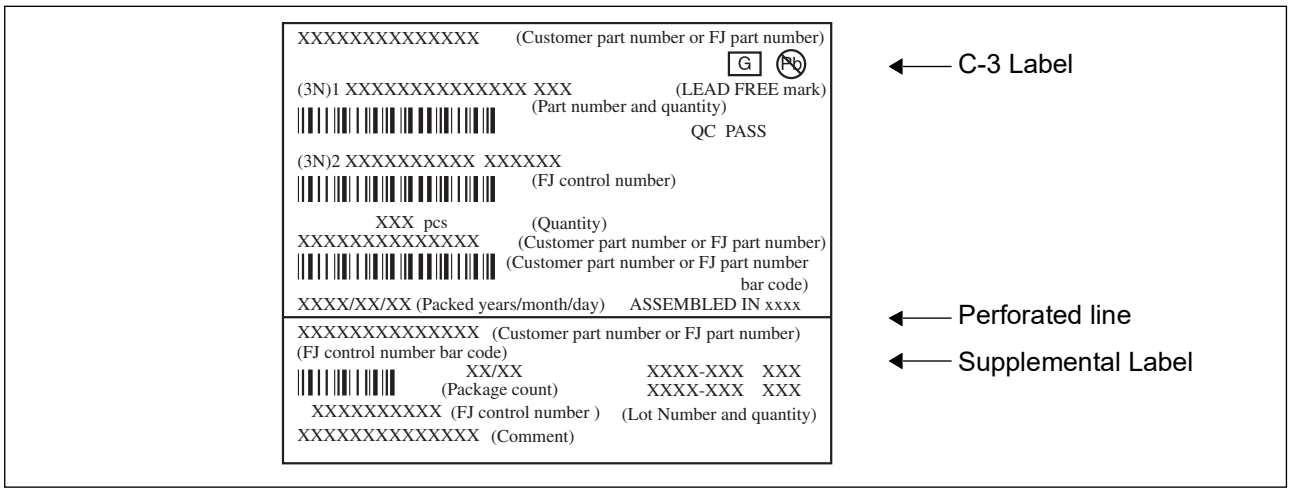


Dimensions in mm

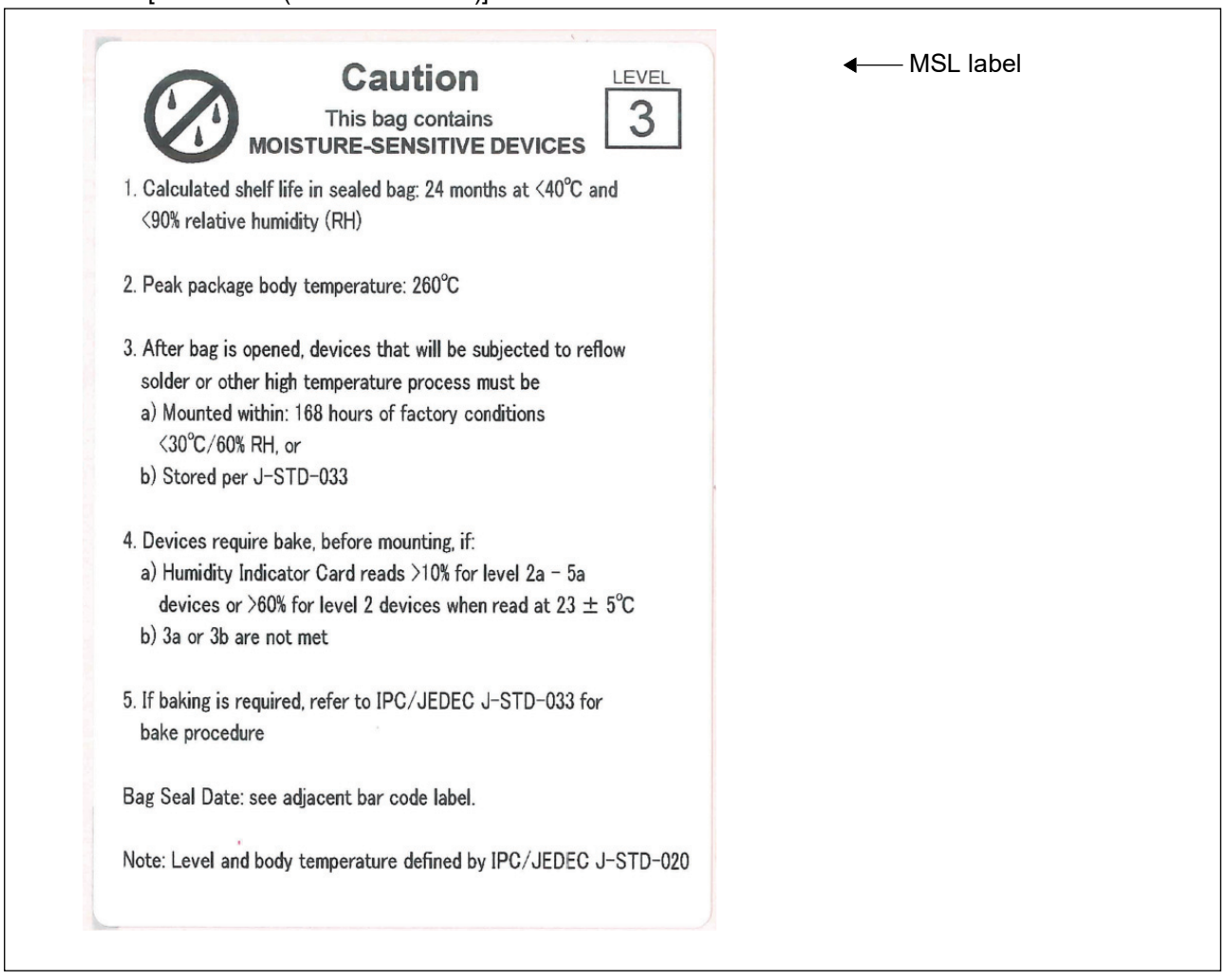
A	B	C	W1	W2
254	100	13	25.5	29.5

2.5 Product label indicators (an example)

Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

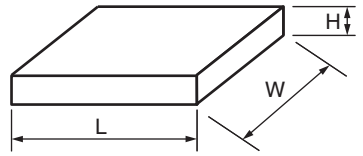


Label II: Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)
[MSL Label (100mm × 70mm)]



2.6 Dimensions for Containers

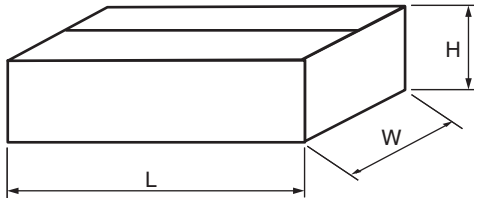
(1) Dimensions for inner box



Tape width	L	W	H
24	265	262	51

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
549	277	180

(Dimensions in mm)

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