ASSP

ISO/IEC 18000-6 Type-C Compliant FeRAM Embedded UHF Band RFID LSI

MB97R8050

■ OVERVIEW

This specification defines physical and logical requirements for the passive RFID Tag LSI “MB97R8050” based on international standard “EPCglobal Class 1 Generation 2 (Ver.1.2.0).

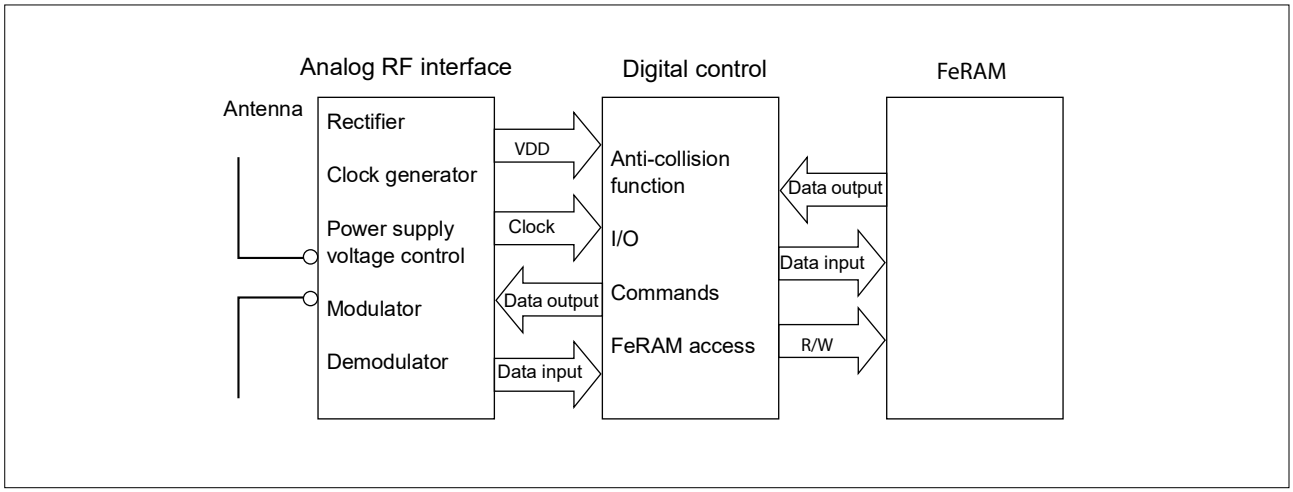
In this document, the term “interrogator” used in the EPCglobal standard is changed to R/W (reader/writer) in accordance with customary practice. The term “Tag” is used as it is.

■ FEATURE

- Compliant with EPCglobal Class 1 Generation 2 (C1G2) Ver.1.2.0
  - Compliant with all UHF bands all over the world (carrier frequency: 860 MHz to 960 MHz)
  - High-speed data transmission (compliant with EPCglobal C1G2)
    R/W → Tag: 26.7 kbps to 128 kbps (when the counts of data 0 and 1are equal)
    Tag → R/W: 40 kbps to 640 kbps
  - DSB-ASK, SSB-ASK, PR-ASK modulation (compliant with EPCglobal C1G2)
  - Anti-collision function
  - Frequency hopping
- FeRAM : High speed read/write Non-volatile memory
  - Read/Write endurance: 10^{10} times
  - Memory data retention: 10years (+ 55 °C)

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited.
RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

■ BLOCK DIAGRAM



■ RF INTERFACE

RF signal interface is compliant with EPCglobal C1G2 Ver.1.2.0 (as described in 6.3.1).

■ MEMORY

1. Memory addressing

Memory addressing uses Extensible bit vectors (EBV) format, which is compliant with EPCglobal C1G2 Ver1.2.0 (Annex A).

2. Memory Map

(1) Memory area

The memory is divided into the following four areas. There is only 48-bit FeRAM in TID area.

- Four memory areas

Name	Memory size	BANK	Address range	Access command
TID	11w × 16b = 176bit	10	00_H to $0A_H$	R/S
EPC	10w × 16b = 160bit	01	00_H to 09_H	R/W/S/BLW/BLE
Reserved	4w × 16b = 64bit	00	00_H to 03_H	R/W
System	1w × 16b = 16bit	—	—	L

Note : Command abbreviation:
R:READ, W: WRITE, S: SELECT, L: Lock, BLW: BlockWrite, BLE: BlockErase

The TID, EPC, and Reserved memory areas contain the data that is defined by the EPCglobal C1G2 specification (Chapter 6.3.2.1). The memory areas are also called as “Memory bank” or “Bank” in EPC standard.

In each memory bank, the logical address starts from zero (00_H).
Logical addressing in EBV-8 format is used.
The system area stores memory lock information.
The memory map is shown in the table on next page. (The system area is not disclosed).

- Memory map

Memory Bank Name	Memory Bank Number	Memory Bank Bit Address	Memory Bank Word Address	Data Description	Size (word)	Total (word)	Total (bit)
TID	10	A0H–AFH	0AH	BlockWrite and BlockErase Segment [15:0]	1	11	176
		90H–9FH	09H	BlockWrite and BlockErase Segment [31:16]	1		
		80H–8FH	08H	BlockWrite and BlockErase Segment [47:32]	1		
		70H–7FH	07H	BlockWrite and BlockErase Segment [63:48]	1		
		60H–6FH	06H	Optional Command Support Segment [15:0]	1		
		50H–5FH	05H	Serial Number Segment [15:0]	1		
		40H–4FH	04H	Serial Number Segment [31:16]	1		
		30H–3FH	03H	Serial Number Segment [47:32]	1		
		20H–2FH	02H	XTID Header Segment [15:0]	1		
		10H–1FH	01H	TAG MDID[3:0], TAG MODEL NUMBER[11:0]	1		
		00H–0FH	00H	E2H, TAG MDID[11:4]	1		
EPC	01	90H–9FH	09H	EPC[15:0]	1	10	160
		80H–8FH	08H	EPC[32:16]	1		
		70H–7FH	07H	EPC[47:32]	1		
		60H–6FH	06H	EPC[63:48]	1		
		50H–5FH	05H	EPC[79:64]	1		
		40H–4FH	04H	EPC[95:80]	1		
		30H–3FH	03H	EPC[111:96]	1		
		20H–2FH	02H	EPC[127:112]	1		
		10H–1FH	01H	StoredPC[15:0]	1		
		00H–0FH	00H	StoredCRC16[15:0]	1		
RESERVED	00	30H–3FH	03H	ACCESS-Password[15:0]	1	4	64
		20H–2FH	02H	ACCESS-Password[31:16]	1		
		10H–1FH	01H	KILL-Password[15:0]	1		
		00H–0FH	00H	KILL-Password[31:16]	1		

(2) TID

This LSI contains 176-bit XTID format data in compliance with EPC Tag Data Standard 1.6 (abbreviated as TDS 1.6 in the following).

XTID consists of the following items. The 8-bit data (00H to 07H) indicates Identifier of EPC with the fixed value of ”E2H”.

- TAG MDID (08H to 13H)
  The 12-bit data indicates IC manufacture code with fixed value of ”810H”.
- TAG MODEL NUMBER (14H to 1FH)
  The unique 12-bit serial number is assigned by Fujitsu Semiconductor.
  The first 8-bit data of TAG MODEL NUMBER [11:4] indicates LSI code with fixed value of “07H”.
  The bottom 4-bit data of TAG MODEL NUMBER [3:0] indicates LSI version.
- XTID Header Segment (20H to 2FH)
  The 16-bit data indicates XTID’s support status with fixed value of “3800H”.
- Serial Number Segment (30H to 5FH)
  The unique 48-bit serial number is assigned by Fujitsu Semiconductor.

- Optional Command Support Segment (60_H to $6F_H$)
  The 16-bit data indicates EPC's maximum size and supported Optional command with fixed value of "$0CC8_H$".
- BlockWrite and BlockErase Segment (70_H to AF_H)
  The 64-bit data indicates the support status of BlockWrite and BlockErase with fixed value of "$0002\_0308\_0002\_0302_H$".

- XTID format

TDS 1.6 Reference Section	TID MEM BANK BIT ADDRESS	BIT ADDRESS WITHIN WORD (In Hexadecimal)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
16.2.4	$A0_H$–AF_H	BlockWrite and BlockErase Segment [15:0]															
	90_H–$9F_H$	BlockWrite and BlockErase Segment [31:16]															
	80_H–$8F_H$	BlockWrite and BlockErase Segment [47:32]															
	70_H–$7F_H$	BlockWrite and BlockErase Segment [63:48]															
16.2.3	60_H–$6F_H$	Optional Command Support Segment [15:0]															
16.2.2	50_H–$5F_H$	Serial Number Segment [15:0]															
	40_H–$4F_H$	Serial Number Segment [31:16]															
	30_H–$3F_H$	Serial Number Segment [47:32]															
16.2.1	20_H–$2F_H$	XTID Header Segment [15:0]															
16.1 and 16.2	10_H–$1F_H$	TAG MDID[3:0]				TAG MODEL NUMBER[11:0]											
	00_H–$0F_H$	$E2_H$								TAG MDID[11:4]							

- XTID format of this LSI

TDS 1.6 Reference Section	TID MEM BANK BIT ADDRESS	BIT ADDRESS WITHIN WORD (In Hexadecimal)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
16.2.4	$A0_H$–AF_H	0302_H															
	90_H–$9F_H$	0002_H															
	80_H–$8F_H$	0308_H															
	70_H–$7F_H$	0002_H															
16.2.3	60_H–$6F_H$	$0CC8_H$															
16.2.2	50_H–$5F_H$	Serial Number Segment [15:0]															
	40_H–$4F_H$	Serial Number Segment [31:16]															
	30_H–$3F_H$	Serial Number Segment [47:32]															
16.2.1	20_H–$2F_H$	3800_H															
16.1 and 16.2	10_H–$1F_H$	0_H				07_H, TAG MODEL NUMBER[3:0]											
	00_H–$0F_H$	$E2_H$								81_H							

(3) EPC

EPC default value consists of the following items.

- EPC Length : 96 bit
- EPC Code : The 48-bit serial number written in TID

EPC Word	EPC BANK BIT ADDRESS	BIT ADDRESS WITHIN WORD (In Hexadecimal)																Description
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
9	90_H – $9F_H$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
8	80_H – $8F_H$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
7	70_H – $7F_H$	Serial Number (TID [15:0])																EPC[15:0]
6	60_H – $6F_H$	Serial Number (TID [31:16])																EPC[31:16]
5	50_H – $5F_H$	Serial Number (TID [47:32])																EPC[47:32]
4	40_H – $4F_H$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPC[63:48]
3	30_H – $3F_H$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPC[79:64]
2	20_H – $2F_H$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPC[95:80]
1	10_H – $1F_H$	Length					UMI	XI	T	Attribute Bits								StoredPC
		0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
0	00_H – $0F_H$	(CRC-16)																StoredCRC

■ FLAGS AND RANDOM NUMBER GENERATOR

The inventoried flag, selected flag, and random number generator are compliant with EPCglobal C1G2 Ver. 1.2.0. (Chapter 6.3.2.2, 6.3.2.3, 6.3.2.5)

■ TAG STATES AND SLOT COUNTER

The Tag states and slot counter are compliant with EPCglobal C1G2 Ver. 1.2.0. (Chapter 6.3.2.4)

■ COLLISION ARBITRATION ALGORITHM

The collision arbitration algorithm is compliant with EPCglobal C1G2 Ver. 1.2.0. (Chapter 6.3.2.6, 6.3.2.7, 6.3.2.8, 6.3.2.9)

■ COMMAND

This LSI supports all mandatory commands and parts of optional commands defined by EPCglobal C1G2 Ver. 1.2.0. (Chapter 6.3.2.11). The commands list and codes are shown in the table below.
For BlockWrite and BlockErase command (Optional command), parts of the specifications are different from the EPC C1G2 standard as described in “(1)BlockWrite (Optional command)” and “(2)BlockErase (Optional command)”.

• Command

Items	Command	Code
Mandatory	QueryRep	00
	ACK	01
	Query	1000
	QueryAdjust	1001
	Select	1010
	NAK	11000000
	Req_RN	11000001
	Read	11000010
	Write	11000011
	Kill	11000100
	Lock	11000101
Optional	Access	11000110
	BlockWrite	11000111
	BlockErase	11001000

• CRC-16(Differences from EPCglobal C1G2 Ver. 1.2.0)

When the R/W writes the entire or part of the PC or EPC area of the Tag, CRC-16 stored in EPC memory 00_H to $0F_H$ of the Tag is disabled until an ACK command is received and a response that is not truncated (PC, EPC, CRC-16) is returned. After the completion of responding to ACK command, the correct CRC-16 value calculated during responding is written to EPC memory (00_H to $0F_H$) as well. If a truncated response to the ACK command is requested before CRC-16 is enabled, the CRC-16 value in the EPC memory, which has not been enabled, is returned as is.

(1) BlockWrite (Optional command; partly supported)

The following table shows the format of the BlockWrite command. Parts of the function of BlockWrite command are different from the EPCglobal C1G2 Ver.1.2.0 as follows.

- MemBank : BlockWrite command can be executed in EPC bank. If BlockWrite command executed to the Reserved bank, the LSI will reply an error code.
- WordCount : If the WordCount is specified over 3 (03_H), the LSI will reply an error code. It can only be specified to 1 (01_H) and 2 (02_H).

- BlockWrite command

	Command	MemBank	WordPtr	WordCount	Data	RN	CRC-16
# of bits	16	2	EBV	8	WordCount × 16	16	16
Description	1100 0111	01: EPC	Starting Address Pointer	Number of word to write	Data to be written	Handle	

(2) BlockErase (Optional command; partly supported)

The following table shows the format of the BlockErase command. Parts function of BlockErase command are different from the EPCglobal C1G2 Ver.1.2.0 as described as follows.

- MemBank : BlockErase command can be executed in EPC bank. If BlockErase executed to the Reserved bank, the LSI will reply an error code.
- WordCount : If the WordCount is specified over 9 (09_H), this LSI will reply an error code. It can only be specified to 8 (08_H) and under except 0 (00_H).

- BlockErase command

	Command	MemBank	WordPtr	WordCount	RN	CRC-16
# of bits	16	2	EBV	8	16	16
Description	1100 1000	01: EPC	Starting Address Pointer	Number of word to erase	Handle	

(3) Error code

The error code is compliant with EPCglobal C1G2 Ver. 1.2.0 (Annex I).

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

Parameter	Symbol	Rating			Unit	Remarks
		Min	Typ	Max		
Maximum input voltage	V_{MAX}	—	—	3.0	V	Between PWRP-PWRM
ESD voltage immunity*	V_{ESD}	− 2	—	+ 2	kV	Human Body Model
		− 100	—	+ 100	V	Machine Model
		− 750	—	+ 750	V	Charged Device Model
Storage temperature	T_{STG}	− 40	—	+ 85	°C	Excluding FeRAM data retention guarantee

* ESD measurement condition: The die chip has been mounted into a QFN40 package.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

2. Recommended Operation Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Operation ambient temperature	Ta	-40	—	+55	°C	
Retention guarantee temperature	Trtn1	-40	—	+55	°C	Retention guarantee period: 10years
Antenna input frequency	Fclk	860	—	960	MHz	According to the Radio Law
Reception modulation depth	(A-B)/A	80	90	100	%	
Data 0 symbol duration	Tari	6.25	—	25	µs	
Receiving waveform rise time	Tr	1	—	500	µs	
Receiving waveform settling time	Ts	—	—	1500	µs	
Receiving waveform fall time	Tf	1	—	500	µs	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

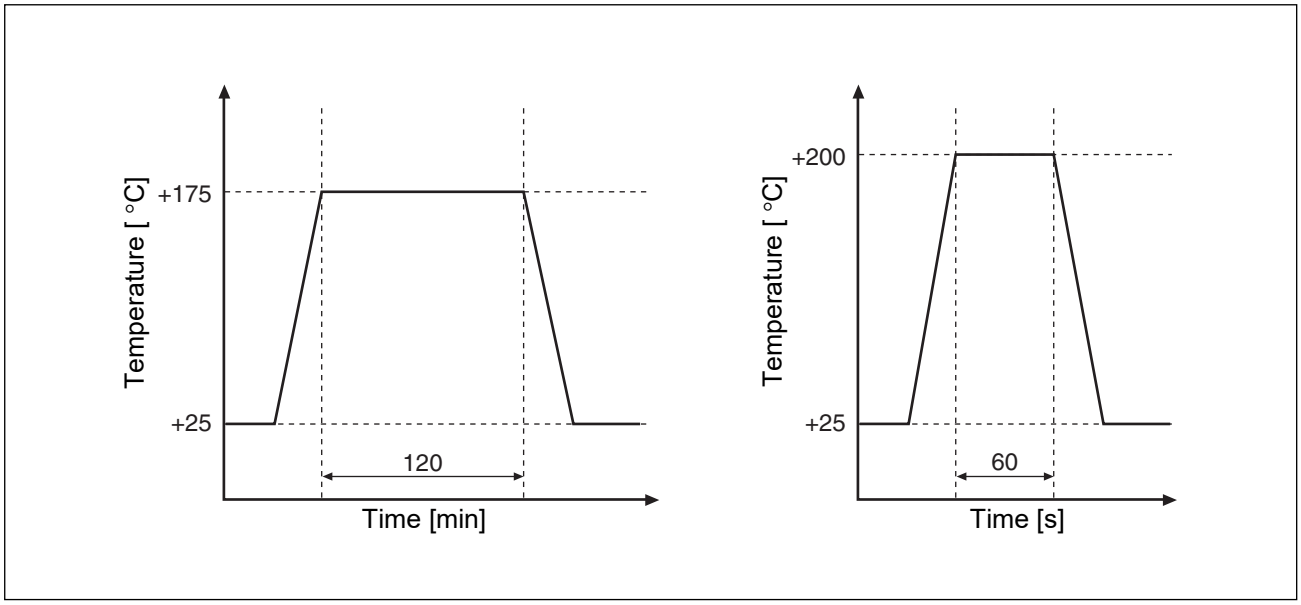
3. RF Communication Characteristics

Parameter	Symbol	Value			Unit	Conditionas/Remarks
		Min	Typ	Max		
Minimum operating power	P_{MIN}	—	−12	—	dBm	Measured by Query Command Tari = 25 μs, BLF = 41kbps, FM0, DSB-ASK, Modulation depth=90%, Ta = 25 °C
Maximum operating power	P_{MAX}		—	20	dBm	
Equivalent input capacitance	C_P	—	0.66	—	pF	Input power = -12 dBm, parallel model (At 920 MHz)
Equivalent input resistance	R_P	—	2.7	—	KΩ	Input power = -12 dBm, parallel model (At 920 MHz)
Receiving bit rate	F_fwd	26.7		128	kbps	PIE code: mark rate = 1/2
Returning bit rate	F_rtrn	40		640	kbps	

■ RECOMMENDED ASSEMBLY CONDITIONS (WAFER)

The MB97R8050 is recommended to be mounted in the following condition to maintain the data retention characteristics of the FeRAM memory when the chip is mounted.

- Mounting temperature of + 175 °C or lower, and 120 minutes or shorter when applied at high temperature, or
- Mounting temperature of + 200 °C or lower, and 60 seconds or shorter when applied at high temperature



■ ORDERING INFORMATION

Part number	Shipping method	Wafer thickness	Remarks
MB97R8050-DIAP15	Wafer (After dicing)	150 μm ± 25.4 μm	

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn left side of that page.

Page	Section	Change Results
—	Overall	Following technical word is revised to more commonly used one. FRAM to FeRAM

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