Memory FeRAM

16 K (2 K × 8) Bit I²C

MB85RC16

■ DESCRIPTION

The MB85RC16 is an FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 2,048 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

Unlike SRAM, the MB85RC16 is able to retain data without using a data backup battery.

The memory cells used in the MB85RC16 have at least 10^{12} Read/Write operation endurance per byte, which is a significant improvement over the number of read/write operations than by other nonvolatile memory products.

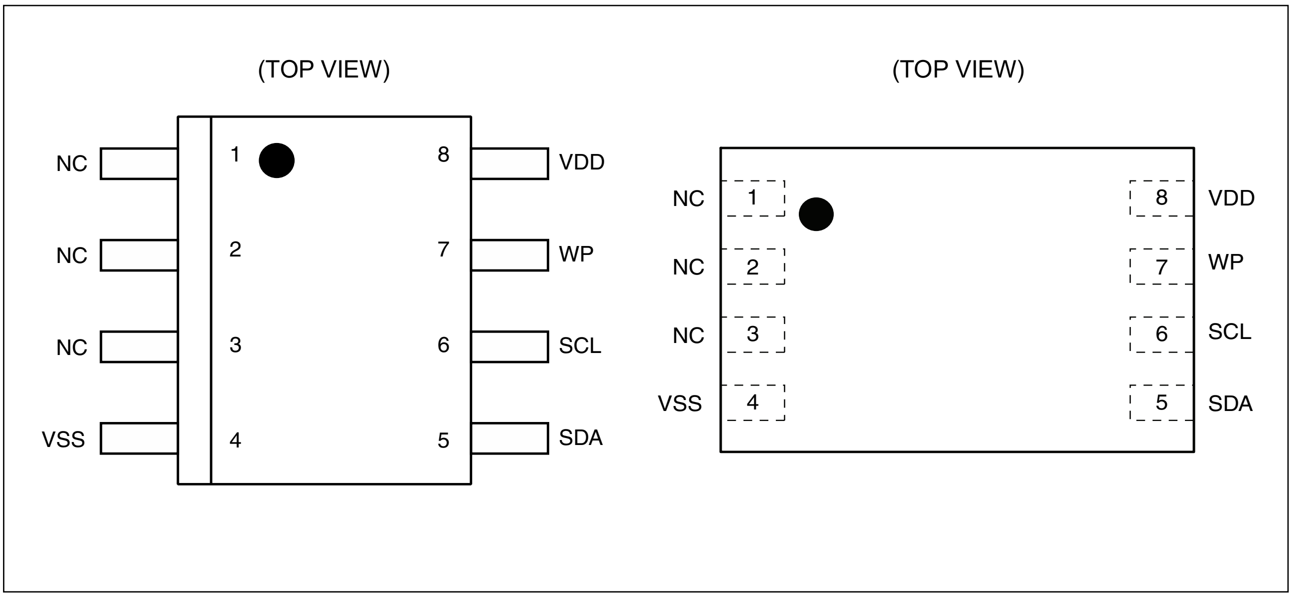
The MB85RC16 can provide writing in one byte units because the long writing time is not required unlike Flash memory and E²PROM. Therefore, the writing completion waiting sequence like a write busy state is not required.

■ FEATURES

• Bit configuration	: 2,048 words × 8 bits
• Two-wire serial interface	: Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
• Operating frequency	: 1 MHz (Max)
• Read/Write endurance	: 10^{12} times/byte
• Data retention	: 10 years (+ 85 °C), 95 years (+ 55 °C), over 200 years (+ 35 °C)
• Operating power supply voltage	: 2.7 V to 3.6 V
• Low power consumption	: Operating power supply current 70 µA (Typ @1 MHz) Standby current 0.1 µA (Typ)
• Operation ambient temperature range	: – 40 °C to + 85 °C
• Package	: 8-pin plastic SOP (FPT-8P-M02) 8-pin plastic SON (LCC-8P-M04) RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited. RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

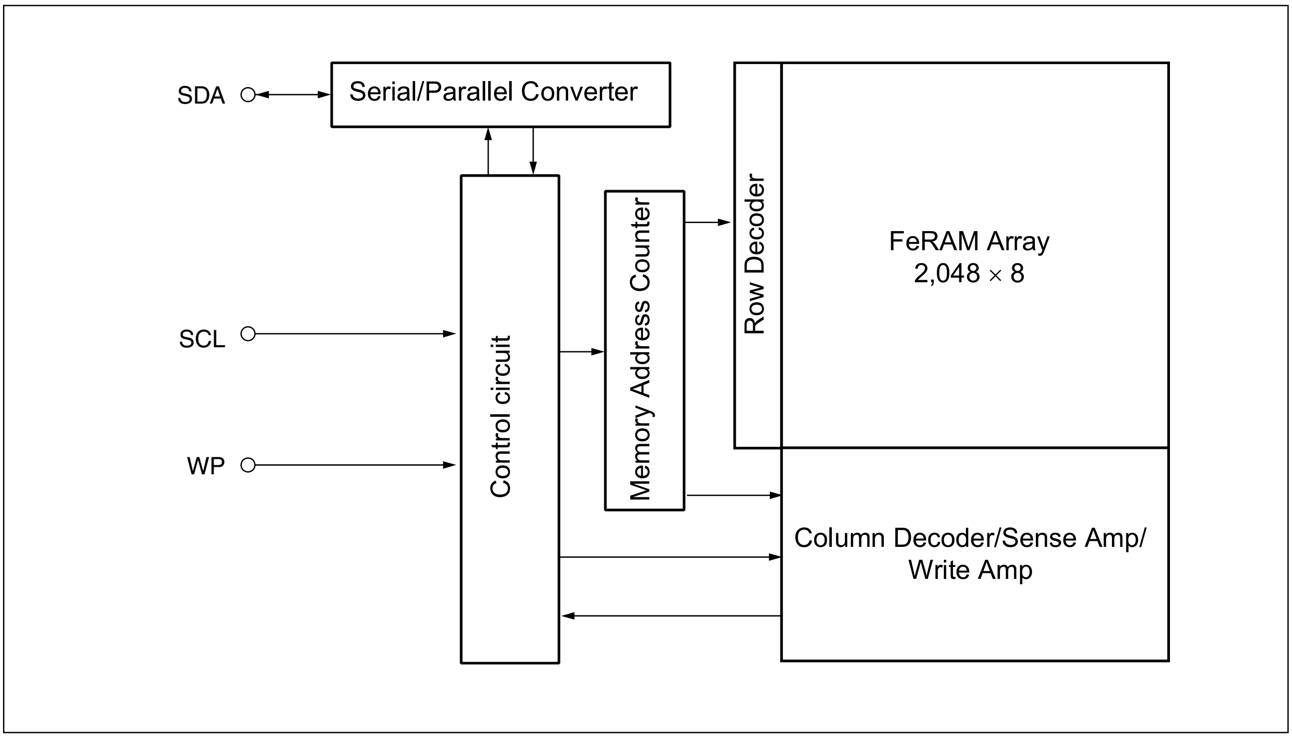
■ PIN ASSIGNMENT



■ PIN FUNCTIONAL DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 3	NC	No Connect pins Leave these pins open, or connect to VDD or VSS.
4	VSS	Ground pin
5	SDA	Serial Data I/O pin This is an I/O pin which performs bidirectional communication for both memory address and writing/reading data. It is possible to connect multiple devices. It is an open drain output, so a pull-up resistor is required to be connected to the external circuit.
6	SCL	Serial Clock pin This is a clock input pin for input/output serial data. Data is sampled on the rising edge of the clock and output on the falling edge.
7	WP	Write Protect pin When the Write Protect pin is the "H" level, the writing operation is disabled. When the Write Protect pin is the "L" level, the entire memory region can be overwritten. The reading operation is always enabled regardless of the Write Protect pin input level. The Write Protect pin is internally pulled down to VSS pin, and that is recognized as the "L" level (write enabled) when the pin is the open state.
8	VDD	Supply Voltage pin

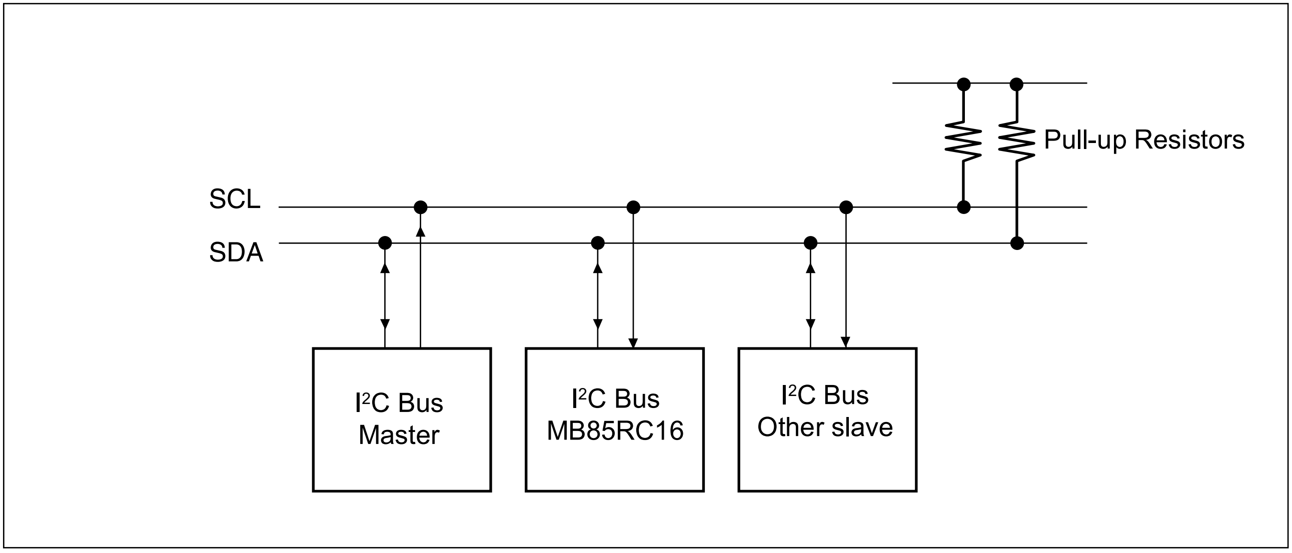
■ BLOCK DIAGRAM



■ I²C (Inter-Integrated Circuit)

The MB85RC16 has the two-wire serial interface; the I²C bus, and operates as a slave device.
The I²C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, an I²C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration.

- **I²C Interface System Configuration Example**



■ I^2C COMMUNICATION PROTOCOL

The I^2C bus provides communication by two wires only, therefore, the SDA input should change while the SCL is the “L” level. However, when starting and stopping the communication sequence, the SDA is allowed to change while the SCL is the “H” level.

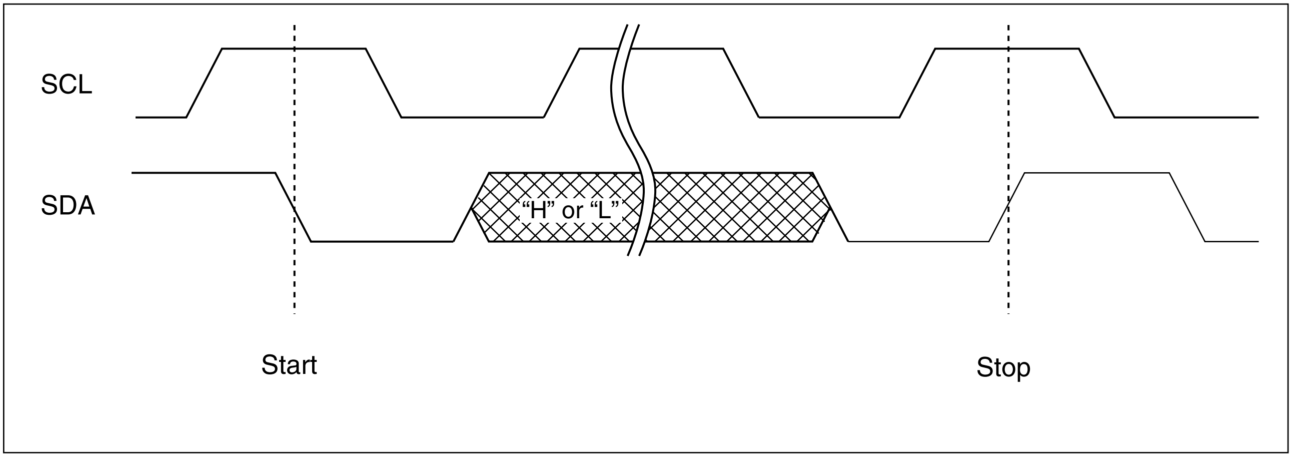
- Start Condition

To start read or write operations by the I^2C bus, change the SDA input from the “H” level to the “L” level while the SCL input is in the “H” level.

- Stop Condition

To stop the I^2C bus communication, change the SDA input from the “L” level to the “H” level while the SCL input is in the “H” level. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data and enters the standby state.

• Start Condition, Stop Condition



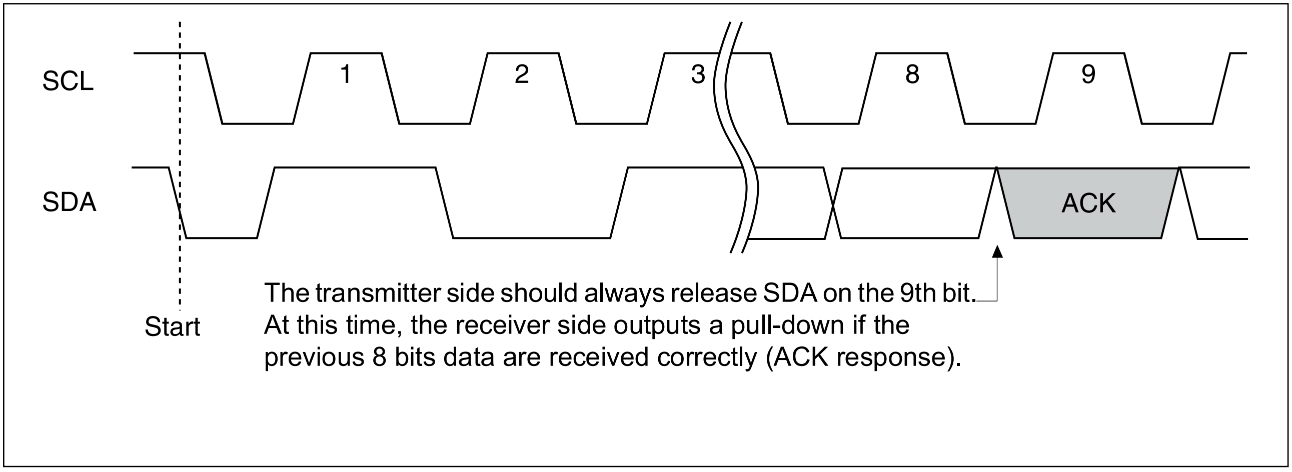
Note : At the write operation, the FeRAM device does not need the programming wait time (t_{WC}) after issuing the Stop Condition.

■ ACKNOWLEDGE (ACK)

In the I²C bus, serial data including memory address or memory information is sent and received in units of 8 bits. The acknowledge signal indicates that every 8 bits of the data is successfully sent and received. The receiver side usually outputs the "L" level every time on the 9th SCL clock after each 8 bits are successfully transmitted and received. On the transmitter side, the bus is temporarily released to Hi-Z every time on this 9th clock to allow the acknowledge signal to be received and checked. During this Hi-Z released period, the receiver side pulls the SDA line down to indicate the "L" level that the previous 8 bits communication is successfully received.

In case the slave side receives Stop condition before sending or receiving the ACK "L" level, the slave side stops the operation and enters to the standby state. On the other hand, the slave side releases the bus state after sending or receiving the NACK "H" level. The master side generates Stop condition or Start condition in this released bus state.

- **Acknowledge timing overview diagram**



The transmitter side should always release SDA on the 9th bit. At this time, the receiver side outputs a pull-down if the previous 8 bits data are received correctly (ACK response).

■ MEMORY ADDRESS STRUCTURE

The MB85RC16 has the memory address buffer to store the 11-bit information for the memory address.

As for byte write, page write and random read commands, the complete 11-bit memory address is configured by inputting the memory upper address (3 bits) and the memory lower address (8 bits), and saved to the memory address buffer. Then access to the memory is performed.

As for a current address read command, the complete 11-bit memory address is configured and saved to the memory address buffer, by inputting the memory upper address (3 bits) and the memory lower address(8 bits) which has saved in the memory address buffer. Then access to the memory is performed.

■ DEVICE ADDRESS WORD

Following the start condition, the 8 bit device address word is input. Inputting the device address word decides whether writing or reading operation. However, the clock is always driven by the master. The device address word (8 bits) consists of a device Type code (4 bits), memory upper address code (3 bits), and a Read/Write code (1 bit).

- Device Type Code (4 bits)

The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at “1010” for the MB85RC16.

- Memory Upper Address Code (3 bits)

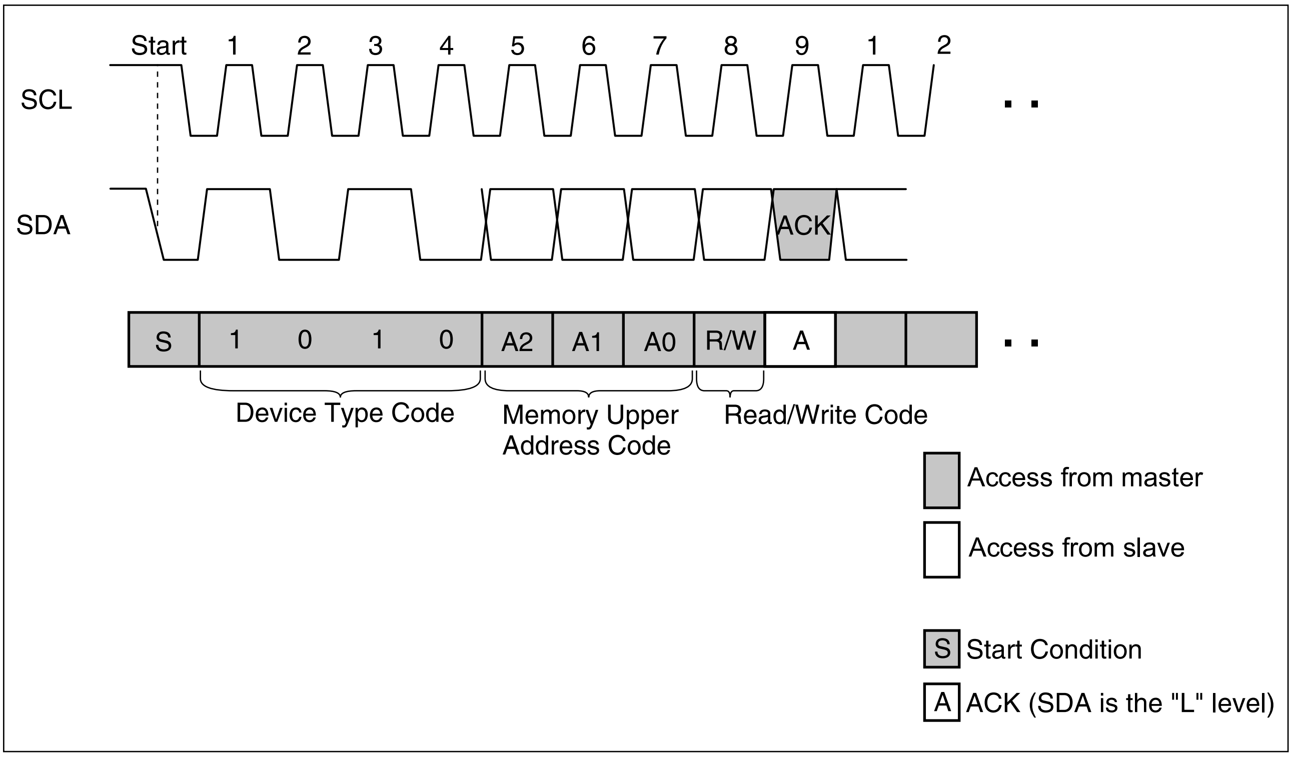
Following the device type code, the 3 bits of the memory upper address code are input.

The slave address selection is not performed by the external pin setting on this device. These 3 bits are not the setting bits for the slave address, but the upper 3-bit setting bits for the memory address.

- Read/Write Code (1 bit)

The 8th bit of the device address word is the R/W (Read/Write) code. When the R/W code is “0” input, a write operation is enabled, and the R/W code is “1” input, a read operation is enabled for the MB85RC16. If the device code is not “1010”, the Read/Write operation is not performed and the standby state is chosen.

• Device Address Word



■ DATA STRUCTURE

The master inputs the device address word (8 bits) following the start condition, and then the slave outputs the Acknowledge “L” level on the 9th bit. After confirming the Acknowledge response, the sequential 8-bit memory lower address is input, to the byte write, page write and random read commands.

As for the current address read command, inputting the memory lower address is not performed, and the address buffer lower 8-bit is used as the memory lower address.

When inputting the memory lower address is finished, the slave outputs the Acknowledge “L” level on the 9th bit again.

Afterwards, the input and the output data continue in 8-bit units, and then the Acknowledge “L” level is output for every 8-bit data.

■ FeRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The MB85RC16 performs the high speed write operations, so any waiting time for an ACK* by the acknowledge polling does not occur.

*: In E^{2}PROM, the Acknowledge Polling is performed as a progress check whether rewriting is executed or not. It is normal to judge by the 9th bit of Acknowledge whether rewriting is performed or not after inputting the start condition and then the device address word (8 bits) during rewriting.

■ WRITE PROTECT (WP)

The entire memory array can be write protected by setting the WP pin to the “H” level. When the WP pin is set to the “L” level, the entire memory array will be rewritten. Reading is allowed regardless of the WP pin's “H” level or “L” level.

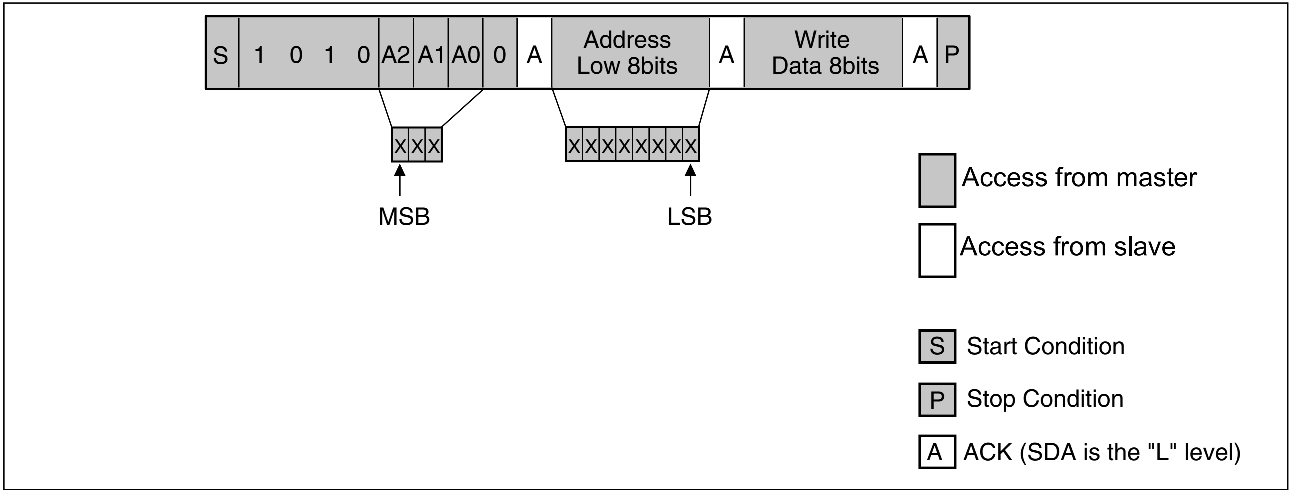
Do not change the WP signal level during the communication period from the start condition to the stop condition.

Note : The WP pin is pulled down internally to VSS pin, therefore if the WP pin is open, the pin status is detected as the “L” level (write enabled).

■ COMMAND

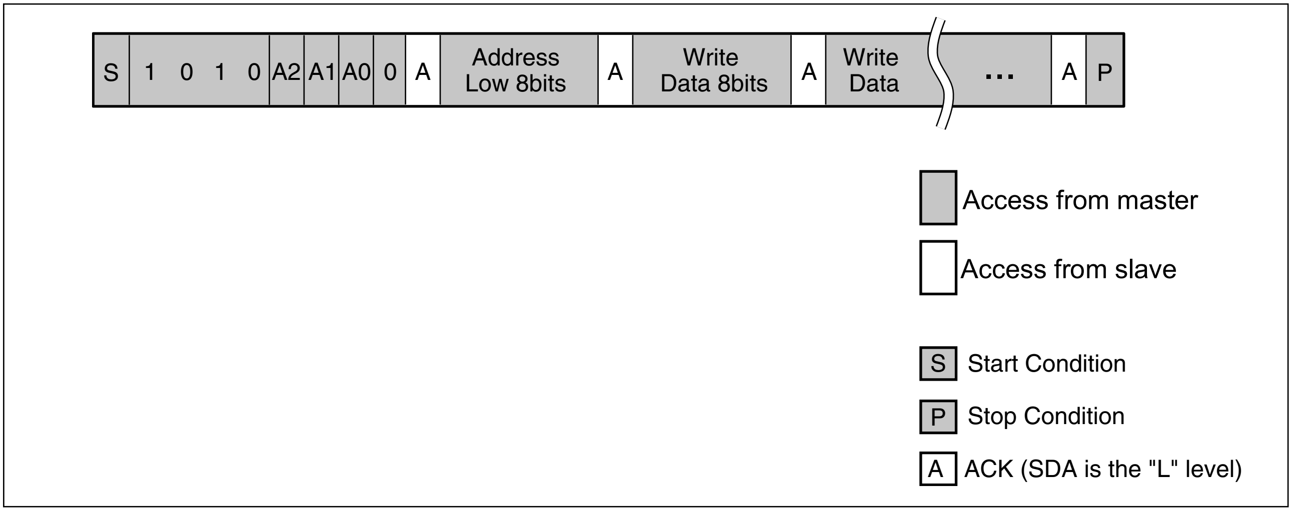
- Byte Write

If the device address word (R/W “0” input) is sent after the start condition, the slave responds with an ACK. After this ACK, write memory addresses and write data are sent in the same way, and the write ends by generating a stop condition at the end.



- Page Write

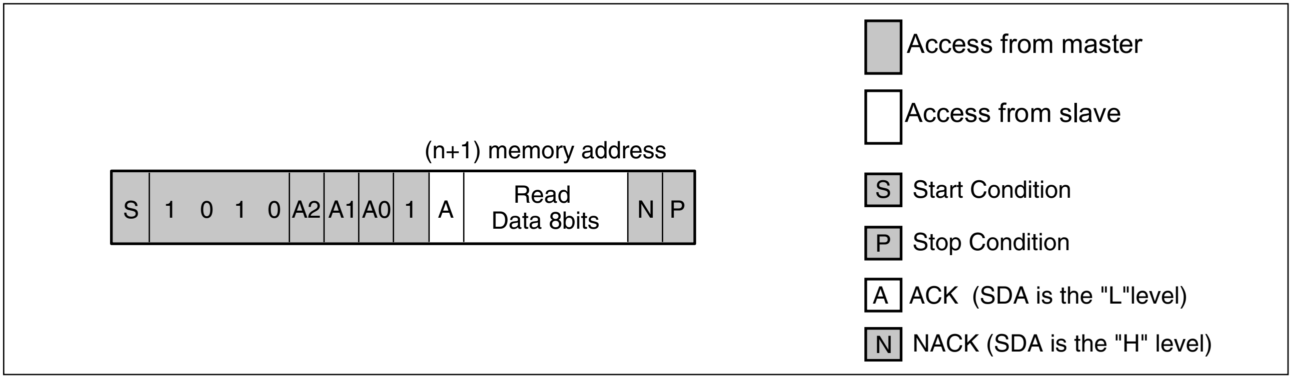
If additional 8 bits are continuously sent after the same command (except stop condition) as Byte Write, a page write is performed. The memory address rolls over to first memory address (000_H) at the end of the address. Therefore, if more than 2 Kbytes are sent, the data is overwritten in order starting from the start of the memory address that was written first.



- Current Address Read

If the last write or read operation finishes successfully up to the end of stop condition, the memory address that was accessed last remains in the memory address buffer (the length is 11 bits).

When sending this command without turning the power off, it is possible to read from the memory address n+1 which adds 1 to the total 11-bit memory address n, which consists of the memory upper address 3-bit from the device address word input and the lower 8-bit of the memory address buffer. If the memory address n is the last address, it is possible to read with rolling over to the head of the memory address (000_H). The current address (address that the memory address buffer indicates) is undefined immediately after turning the power on.

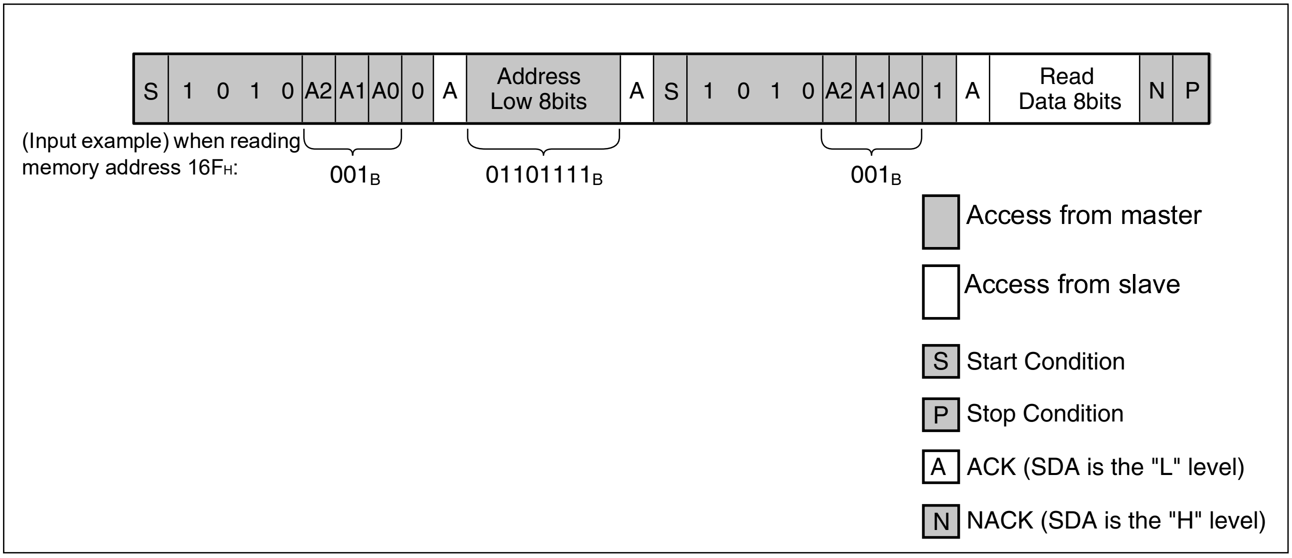


- Random Read

The one byte of data from the memory address saved in the memory address buffer can be read out synchronously to SCL by specifying the address in the same way as for a write, and then issuing another start condition and sending the Device Address Word (R/W “1” input).

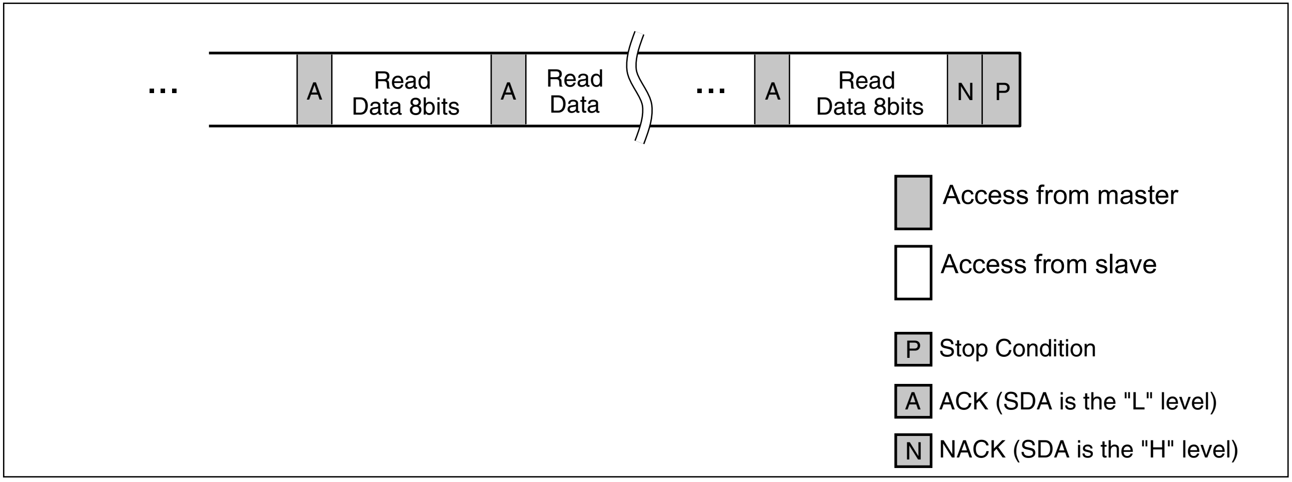
Setting values for the first and the second memory upper address codes should be the same (an example is shown in below).

The final NACK (SDA is the “H” level) is issued by the receiver that receives the data. In this case, this bit is issued by the master side.



- Sequential Read

Data can be received continuously following the Device address word (R/W “1” input) after specifying the address in the same way as for Random Read. If the read reaches the end of address, the read address automatically rolls over to first memory address (000H) and keeps reading.

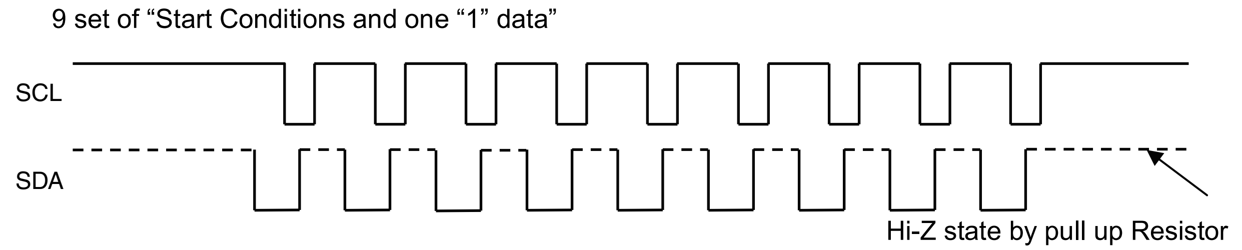


■ SOFTWARE RESET SEQUENCE OR COMMAND RETRY

In case the malfunction has occurred after power on, the master side stopped the I²C communication during processing, or unexpected malfunction has occurred, execute the following (1) software recovery sequence just before each command, or (2) retry command just after failure of each command.

(1) Software Reset Sequence

Since the slave side may be outputting “L” level, do not force to drive “H” level, when the master side drives the SDA port. This is for preventing a bus conflict. The additional hardware is not necessary for this software reset sequence.



Send “Start Condition and one data “1””.
Repeat these 9 times just before Write or Read command.

(2) Command Retry

Command retry is useful to recover from failure response during I²C communication.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	– 0.5	+ 4.0	V
Input voltage*	V_{IN}	– 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Output voltage*	V_{OUT}	– 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Operation ambient temperature	T_A	– 40	+ 85	°C
Storage temperature	Tstg	– 55	+ 125	°C

*: These parameters are based on the condition that VSS is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage[*1]	V_{DD}	2.7	3.3	3.6	V
Operation ambient temperature[*2]	T_A	– 40	—	+ 85	°C

*1: These parameters are based on the condition that VSS is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current*1	$\|I_{LI}\|$	V_{IN} = 0 V to V_{DD}	—	—	1	μA
Output leakage current*2	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{DD}	—	—	1	μA
Operating power supply current	I_{DD}	SCL = 400 kHz	—	30	—	μA
		SCL = 1 MHz	—	70	100	μA
Standby current	I_{SB}	SCL, SDA = V_{DD} WP = 0V or V_{DD} or OPEN T_A = + 25 °C	—	0.1	1	μA
"H" level input voltage	V_{IH}	V_{DD} = 2.7 V to 3.6 V	$V_{DD} \times 0.8$	—	$V_{DD} + 0.5$ (≤ 4.0)	V
"L" level input voltage	V_{IL}	V_{DD} = 2.7 V to 3.6 V	− 0.5	—	+ 0.6	V
"L" level output voltage	V_{OL}	I_{OL} = 3 mA	—	—	0.4	V
Input resistance for WP pin	R_{IN}	V_{IN} = V_{IL} (Max)	50	—	—	kΩ
		V_{IN} = V_{IH} (Min)	1	—	—	MΩ

*1: Applicable pin: SCL,SDA

*2: Applicable pin: SDA

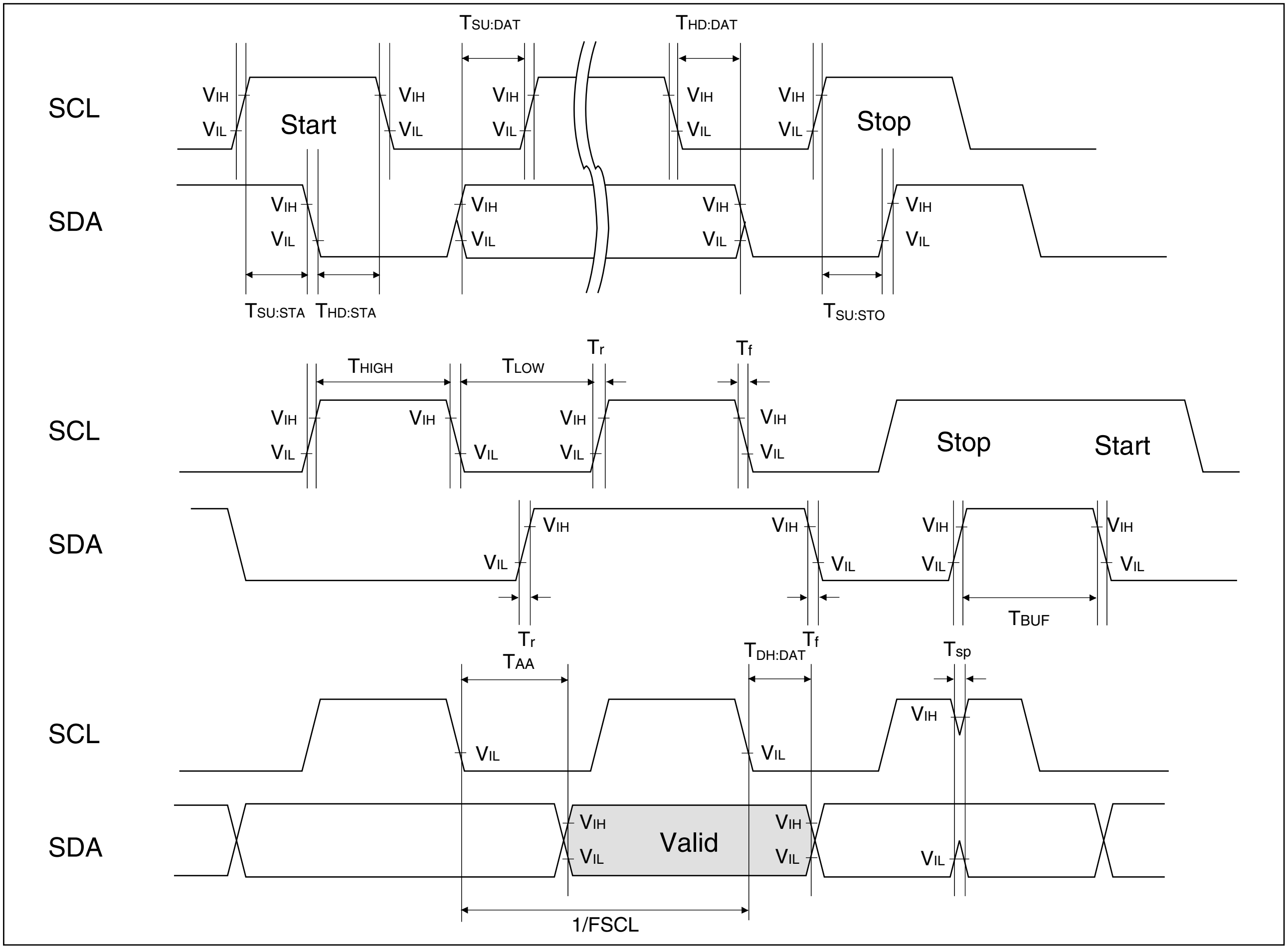
2. AC Characteristics

Parameter	Symbol	Value						Unit
		Standard Mode		Fast Mode		Fast Mode Plus		
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	FSCL	0	100	0	400	0	1000	kHz
Clock high time	T_{HIGH}	4000	—	600	—	400	—	ns
Clock low time	T_{LOW}	4700	—	1300	—	600	—	ns
SCL/SDA rising time	T_r	—	1000	—	300	—	300	ns
SCL/SDA falling time	T_f	—	300	—	300	—	100	ns
Start condition hold	$T_{HD:STA}$	4000	—	600	—	250	—	ns
Start condition setup	$T_{SU:STA}$	4700	—	600	—	250	—	ns
SDA input hold	$T_{HD:DAT}$	20	—	20	—	20	—	ns
SDA input setup	$T_{SU:DAT}$	250	—	100	—	100	—	ns
SDA output hold	$T_{DH:DAT}$	0	—	0	—	0	—	ns
Stop condition setup	$T_{SU:STO}$	4000	—	600	—	250	—	ns
SDA output access after SCL falling	T_{AA}	—	3000	—	900	—	550	ns
Pre-charge time	T_{BUF}	4700	—	1300	—	500	—	ns
Noise suppression time (SCL and SDA)	T_{SP}	—	50	—	50	—	50	ns

AC characteristics were measured under the following measurement conditions.

Power supply voltage : 2.7 V to 3.6 V
Operation ambient temperature : – 40 °C to + 85 °C
Input voltage amplitude : 0.3 V to 2.7 V
Input rising time : 5 ns
Input falling time : 5 ns
Input judge level : $V_{DD}/2$
Output judge level : $V_{DD}/2$

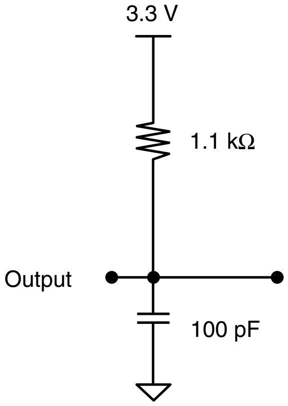
3. AC Timing Definitions



4. Pin capacitance

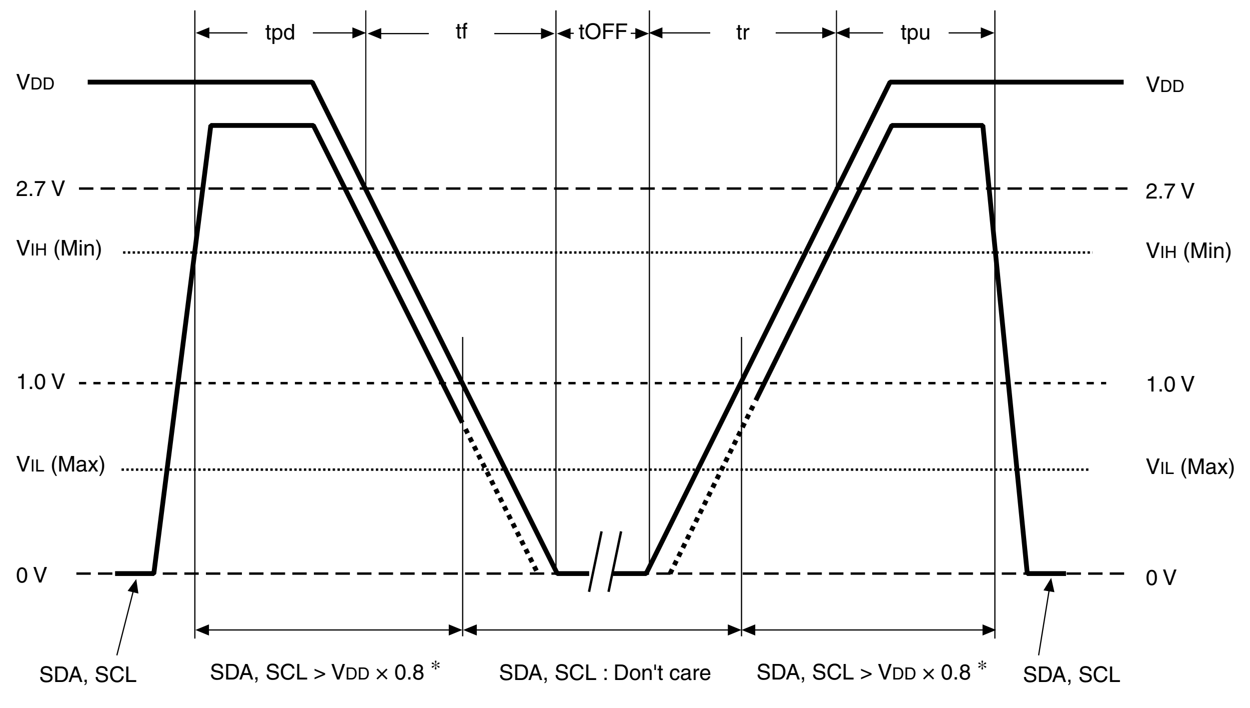
Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
I/O capacitance	$C_{I/O}$	$V_{DD} = V_{IN} = V_{OUT} = 0$ V, f = 1 MHz, $T_A = +25$ °C	—	—	15	pF
Input capacitance	C_{IN}		—	—	15	pF

5. AC Test Load Circuit



■ POWER ON/OFF SEQUENCE

If V_{DD} falls down below 2.0V, V_{DD} is required to be started from 0V to prevent malfunctions when the power is turned on again.



* : SDA, SCL (Max) < V_{DD} + 0.5 V

Parameter	Symbol	Value		Unit
		Min	Max	
SDA, SCL level hold time during power down	tpd	85	—	ns
SDA, SCL level hold time during power up	tpu	85	—	ns
Power supply rising time	tr	0.01	50	ms
Power supply falling time	tf	0.01	50	ms
Power off time	tOFF	50	—	ms

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FeRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10^{12}	—	Times/byte	Operation Ambient Temperature T_A = + 85 °C
Data Retention*2	10	—	Years	Operation Ambient Temperature T_A = + 85 °C
	95	—		Operation Ambient Temperature T_A = + 55 °C
	≥ 200	—		Operation Ambient Temperature T_A = + 35 °C

*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

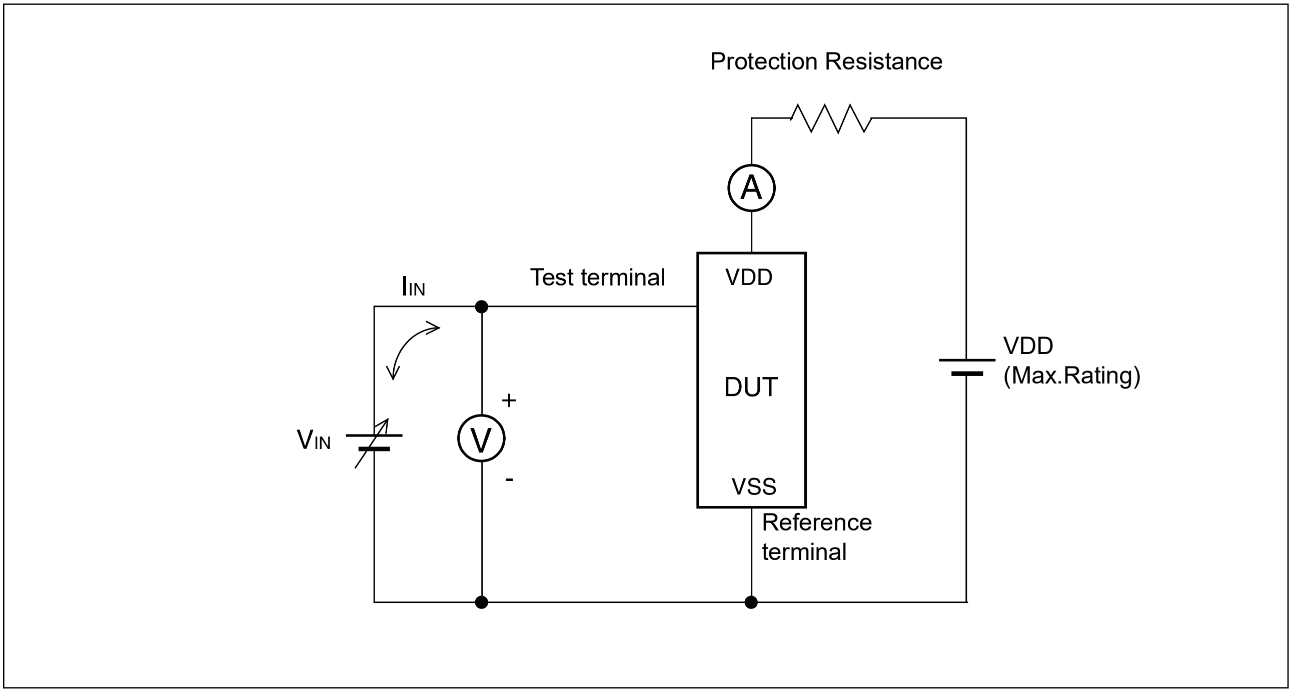
■ NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

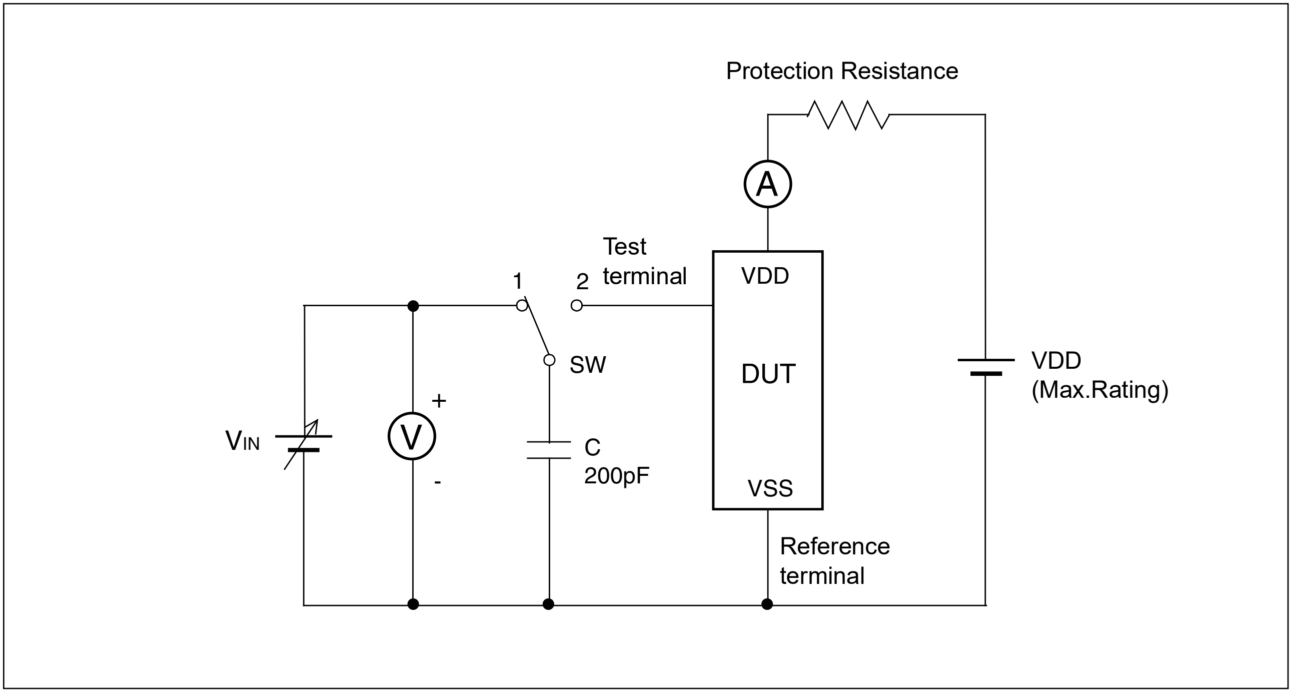
Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RC16PNF-G-JNE1 MB85RC16PNF-G-JNERE1 MB85RC16PNF-G-AME2 MB85RC16PNF-G-AMERE2 MB85RC16PN-G-AMERE1	≥ |2000 V|
ESD MM (Machine Model) JESD22-A115 compliant		≥ |200 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		≥ |1000 V|
Latch-Up (I-test) JESD78 compliant		—
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		≥ |300 mA|
Latch-Up (C-V Method) Proprietary method		—

- Current method of Latch-Up Resistance Test



Note : The voltage V_{IN} is increased gradually and the current I_{IN} of 300 mA at maximum shall flow. Confirm the latch up does not occur under I_{IN} = ± 300 mA. In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

- C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

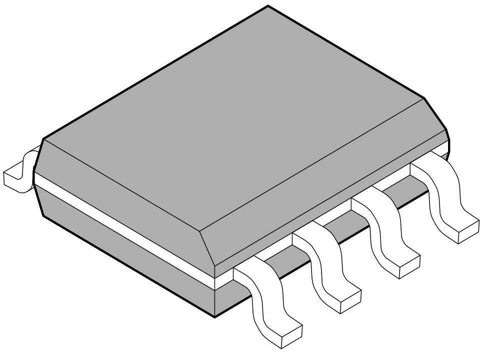
■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RC16PNF-G-JNE1	8-pin, plastic SOP	Tube	—*
MB85RC16PNF-G-JNERE1	8-pin, plastic SOP	Embossed Carrier tape	1500
MB85RC16PNF-G-AME2	8-pin, plastic SON	Tray	—*
MB85RC16PNF-G-AMERE2	8-pin, plastic SON	Embossed Carrier tape	1500
MB85RC16PN-G-AMERE1	8-pin, plastic SON	Embossed Carrier tape	1500

*: Please contact our sales office about minimum shipping quantity.

■ PACKAGE DIMENSION

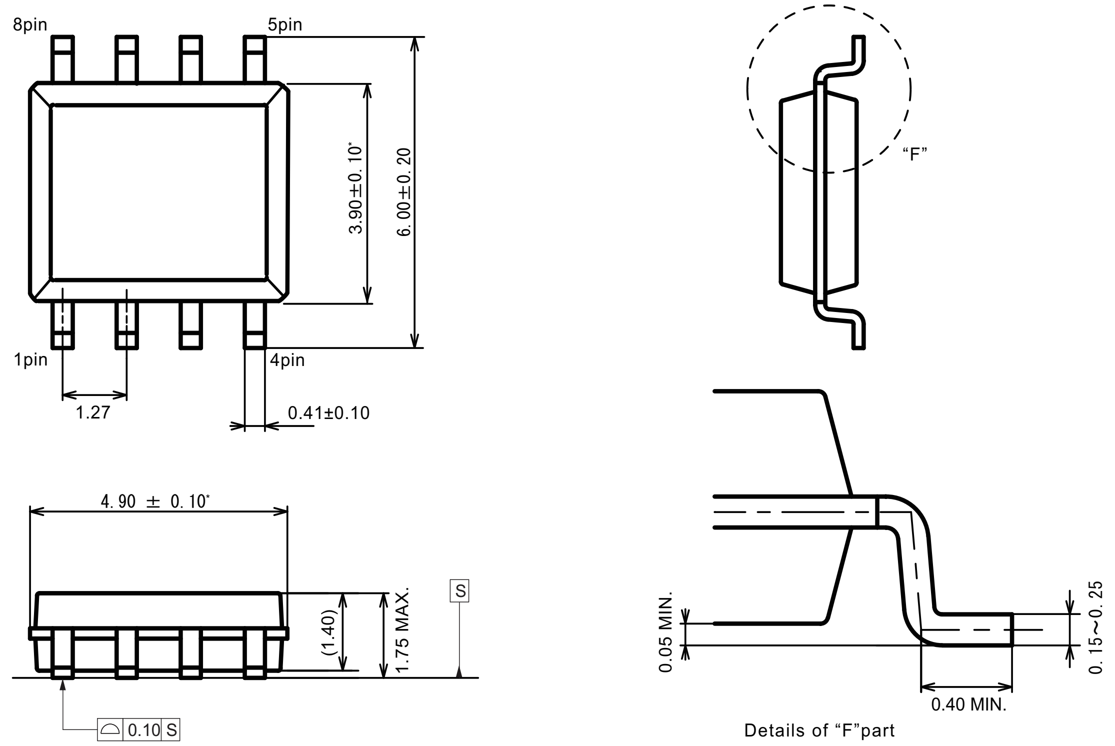
8-pin plastic SOP(150mil)



Lead pitch	1.27mm
Package width x Package length	3.90mm x 4.90mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.75mm MAX.

8-pin plastic SOP

Note *: These dimension do not include resin protrution.
Pins width do not include tie bar cutting remaindar.



Dimension in mm

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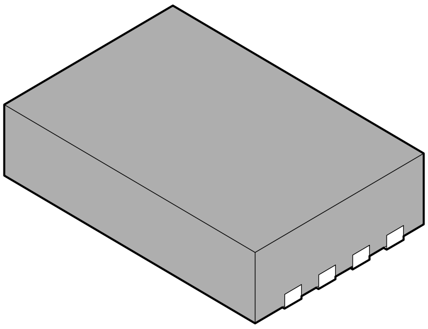
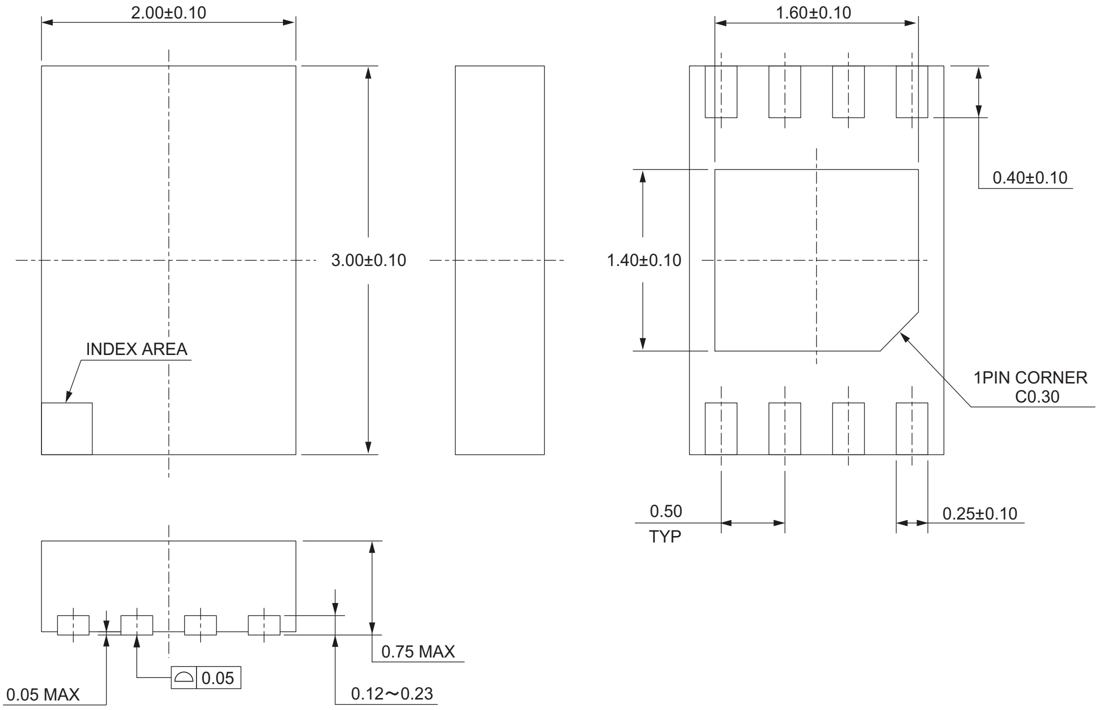
8-pin plastic SON 	Lead pitch	0.50 mm
	Package width × package length	2.00 mm × 3.00 mm
	Sealing method	Plastic mold
	Mounting height	0.75 mm MAX

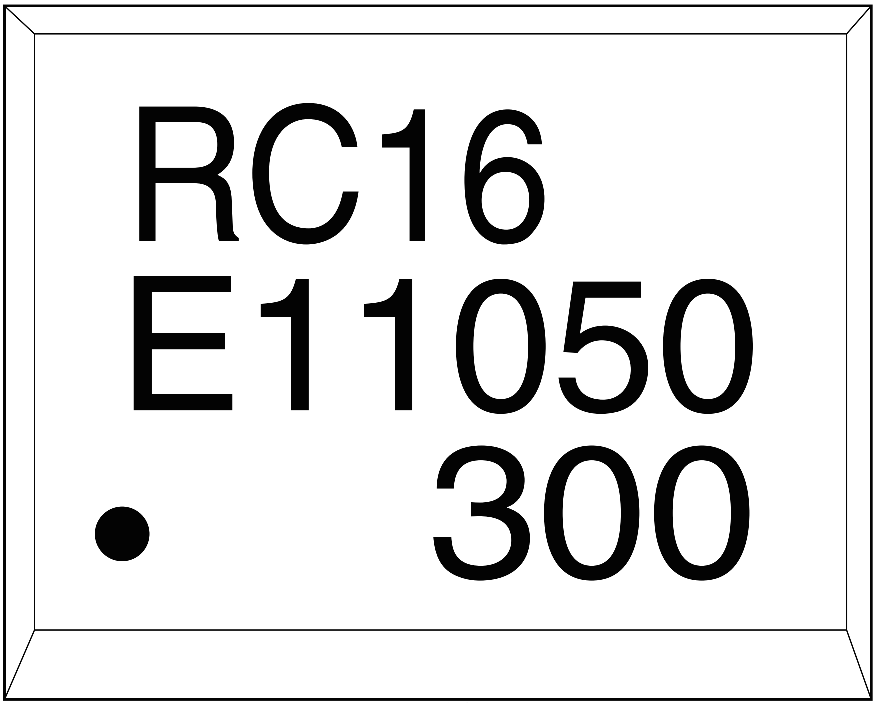
8-pin plastic SON



Dimensions in mm.

■ MARKING

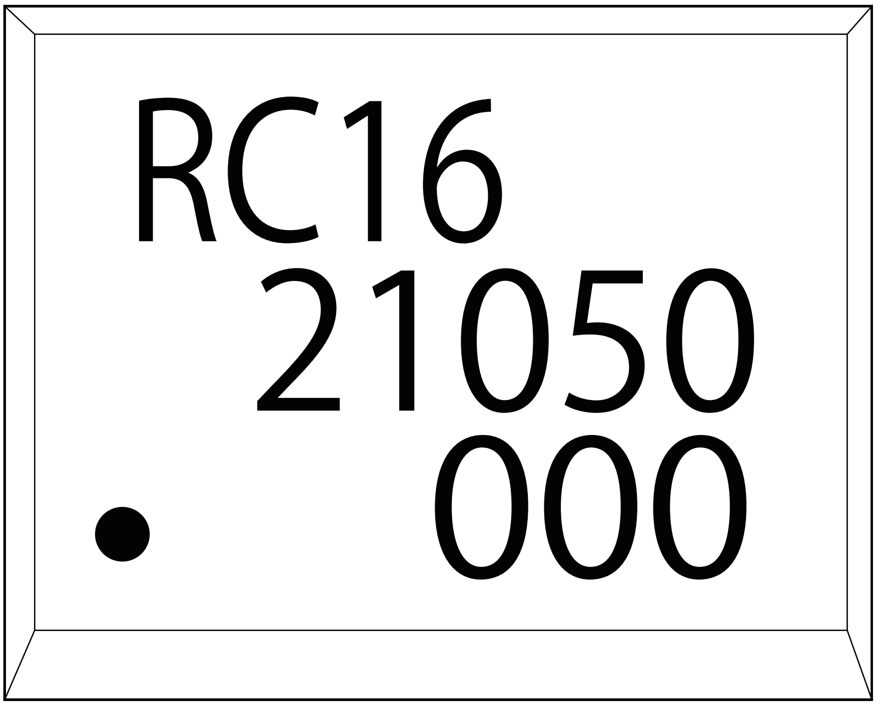
[MB85RC16PNF-G-JNE1]
[MB85RC16PNF-G-JNERE1]



[8-pin plastic SOP, 150mil]

RC16: Product name
E11050: E1(Lead free code) + 1050(Year and Week code)
300: Trace code:

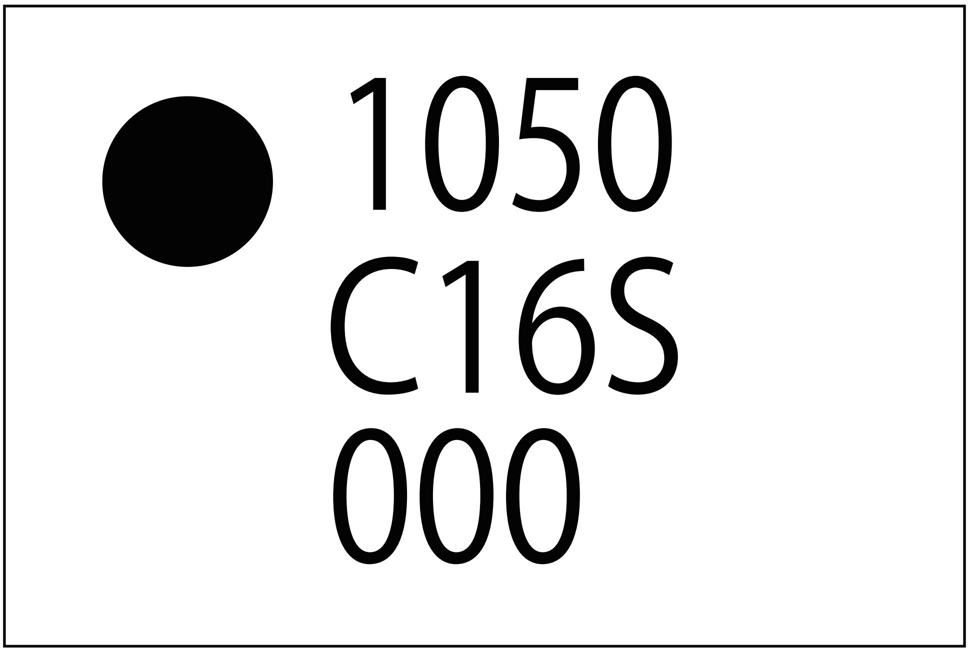
[MB85RC16PNF-G-AME2]
[MB85RC16PNF-G-AMERE2]



[8-pin plastic SOP, 150mil]

RC16: Product name
21050: 2(Lead free code) + 1050(Year and Week code)
000: Trace code:

[MB85RC16PN-G-AMERE1]



[8-pin plastic SON]

1050: Year and Week code
C16S: Product name
000: Trace code:

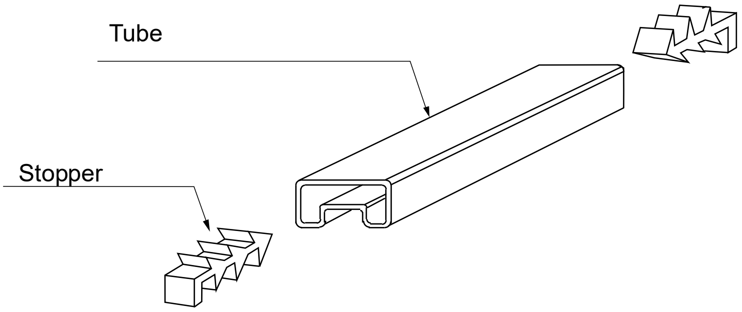
■ PACKING INFORMATION

(1)MB85RC16PNF-G-JNE1/MB85RC16PNF-G-JNERE1/MB85RC16PNF-G-AMERE2/
MB85RC16PNF-G-AME2

1. Tube(MB85RC16PNF-G-JNE1)

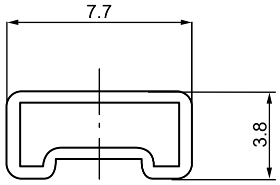
1.1 Tube Dimensions

- Tube/stopper shape (example)



Tube cross-sections and Maximum quantity

MB85RC16PNF-G-JNE1	Maximum quantity		
	ICs/tube	ICs/inner box	ICs/outer box
	95	7,600	30,400

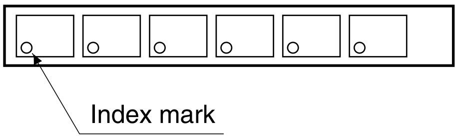


tube length:521

No heat resistance
Package should not be baked by using tube.

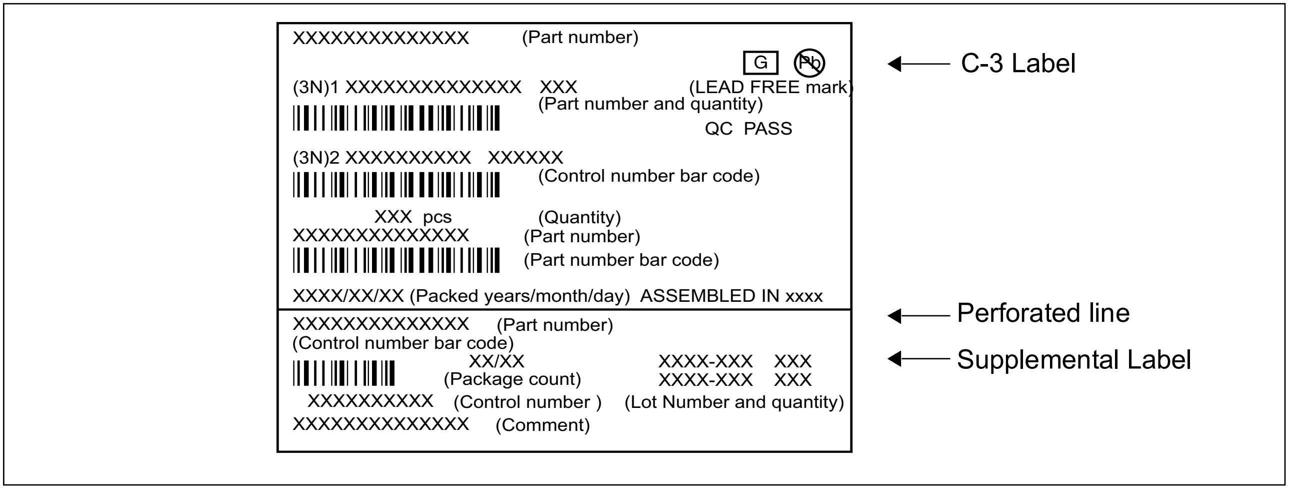
(Dimensions in mm)

- Direction of index in tube



1.2 Product label indicators (an example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



XXXXXXXXXXXXXX (Part number)

G Pb

(3N)1 XXXXXXXXXXXXXX XXX (LEAD FREE mark)
(Part number and quantity)

QC PASS

(3N)2 XXXXXXXXXX XXXXXX
(Control number bar code)

XXX pcs (Quantity)
XXXXXXXXXXXXXX (Part number)
(Part number bar code)

XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx

XXXXXXXXXXXXXX (Part number)
(Control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (Control number) (Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)

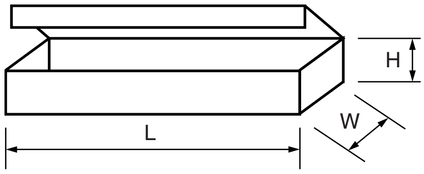
C-3 Label

Perforated line

Supplemental Label

1.3 Dimensions for Containers

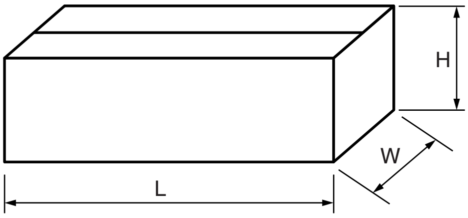
(1) Dimensions for inner box



L	W	H
540	125	75

(Dimensions in mm)

(2) Dimensions for outer box



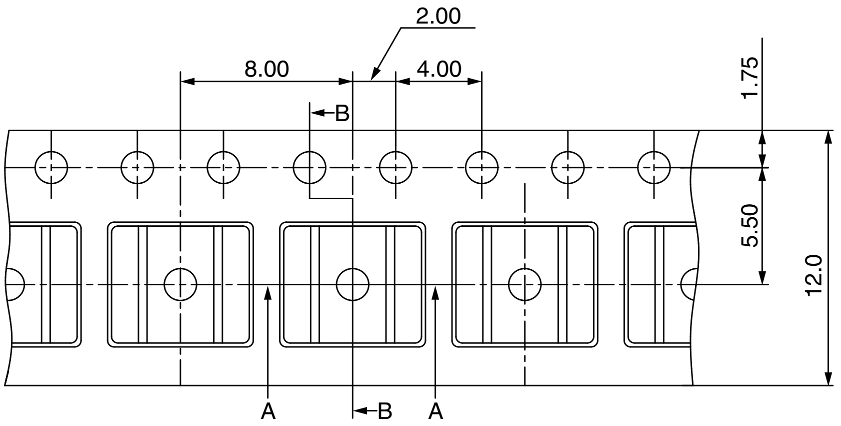
L	W	H
565	270	180

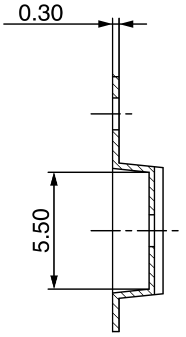
(Dimensions in mm)

2. Emboss Tape(MB85RC16PNF-G-JNERE1/MB85RC16PNF-G-AMERE2)

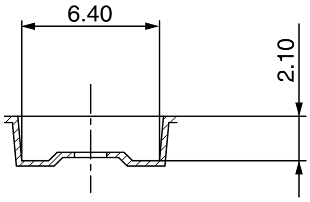
2.1 Tape Dimensions (not drawn to scale) (8-pin plastic SOP 150mil)

Part number	reel diameter	Maximum storage capacity		
		ICs/reel	ICs/inner box	ICs/outer box
MB85RC16PNF-G-JNERE1	φ330	1,500	1,500 (1 pack/inner box)	10,500 (7 inner boxes/ outer box:Max.)
MB85RC16PNF-G-AMERE2	φ254	1,500	1,500 (1 pack/inner box)	9,000 (6 inner boxes/ outer box:Max.)





SEC.B-B

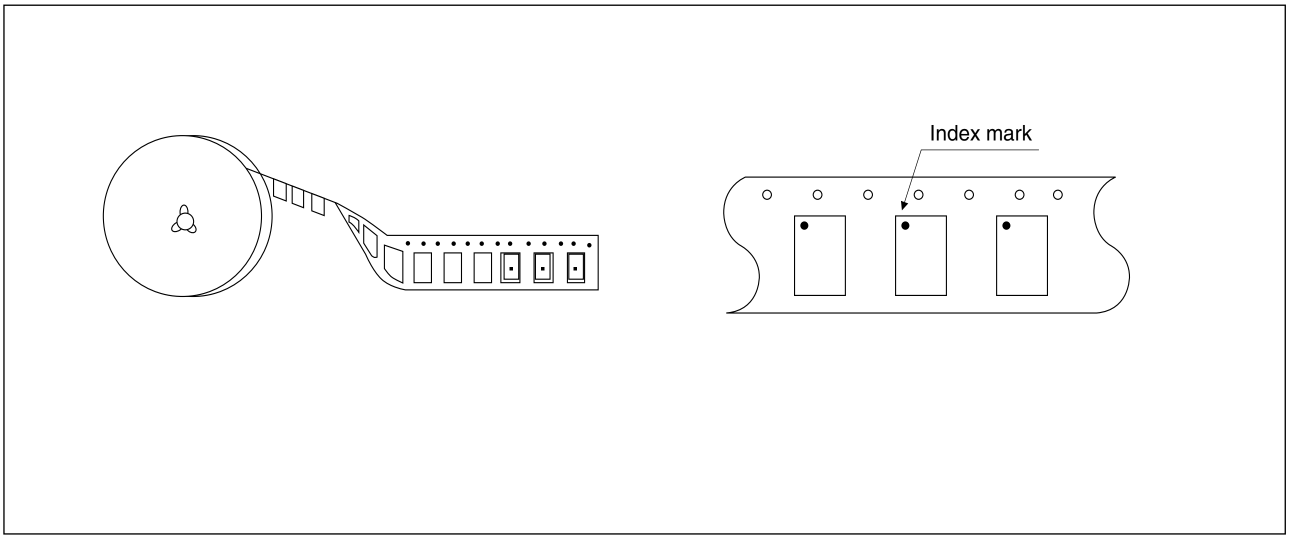


SEC.A-A

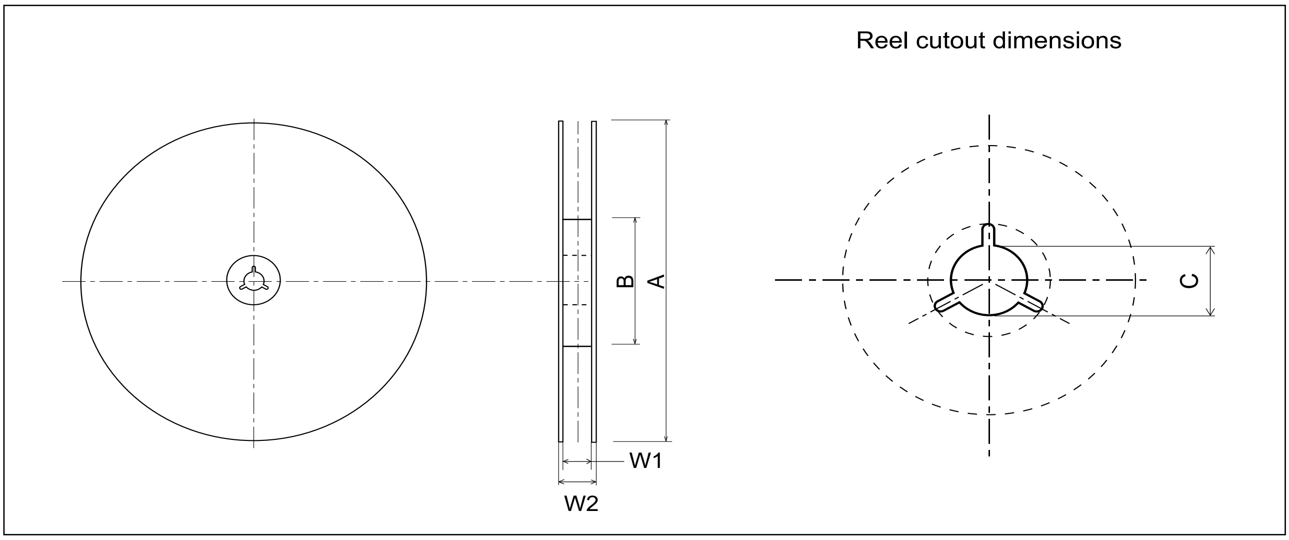
(Dimensions in mm)

Heat proof temperature : No heat resistance.
Package should not be baked by using tape and reel.

2.2 IC orientation



2.3 Reel dimensions

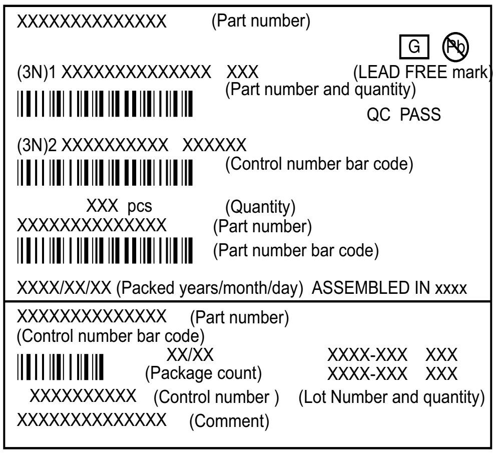


単位：mm

型格	A	B	C	W1	W2
MB85RC16PNF-G-JNERE1	330	100	13	12.4	17.2
MB85RC16PNF-G-AMERE2	254	100	13	13.5	17.5

2.4 Product label indicators (an example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



XXXXXXXXXXXXXX (Part number)

G (LEAD FREE mark)

(3N)1 XXXXXXXXXXXXXX XXX (Part number and quantity)

QC PASS

(3N)2 XXXXXXXXXX XXXXXX (Control number bar code)

XXX pcs (Quantity)

XXXXXXXXXXXXXX (Part number)

(Part number bar code)

XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx

XXXXXXXXXXXXXX (Part number)

(Control number bar code)

XX/XX (Package count)

XXXX-XXX XXX

XXXX-XXX XXX

XXXXXXXXXX (Control number) (Lot Number and quantity)

XXXXXXXXXXXXXX (Comment)

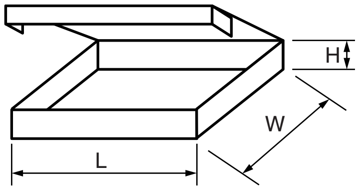
C-3 Label

Perforated line

Supplemental Label

2.5 Dimensions for Containers

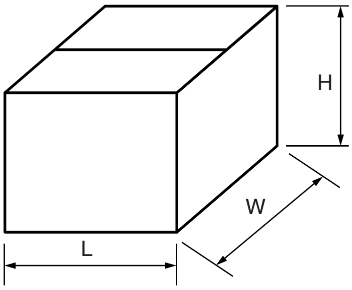
(1) Dimensions for inner box



Part Number	L	W	H
MB85RC16PNF-G-JNERE1	365	345	40
MB85RC16PNF-G-AMERE2	265	260	50

(Dimensions in mm)

(2) Dimensions for outer box



Part Number	L	W	H
MB85RC16PNF-G-JNERE1	415	400	315
MB85RC16PNF-G-AMERE2	565	270	180

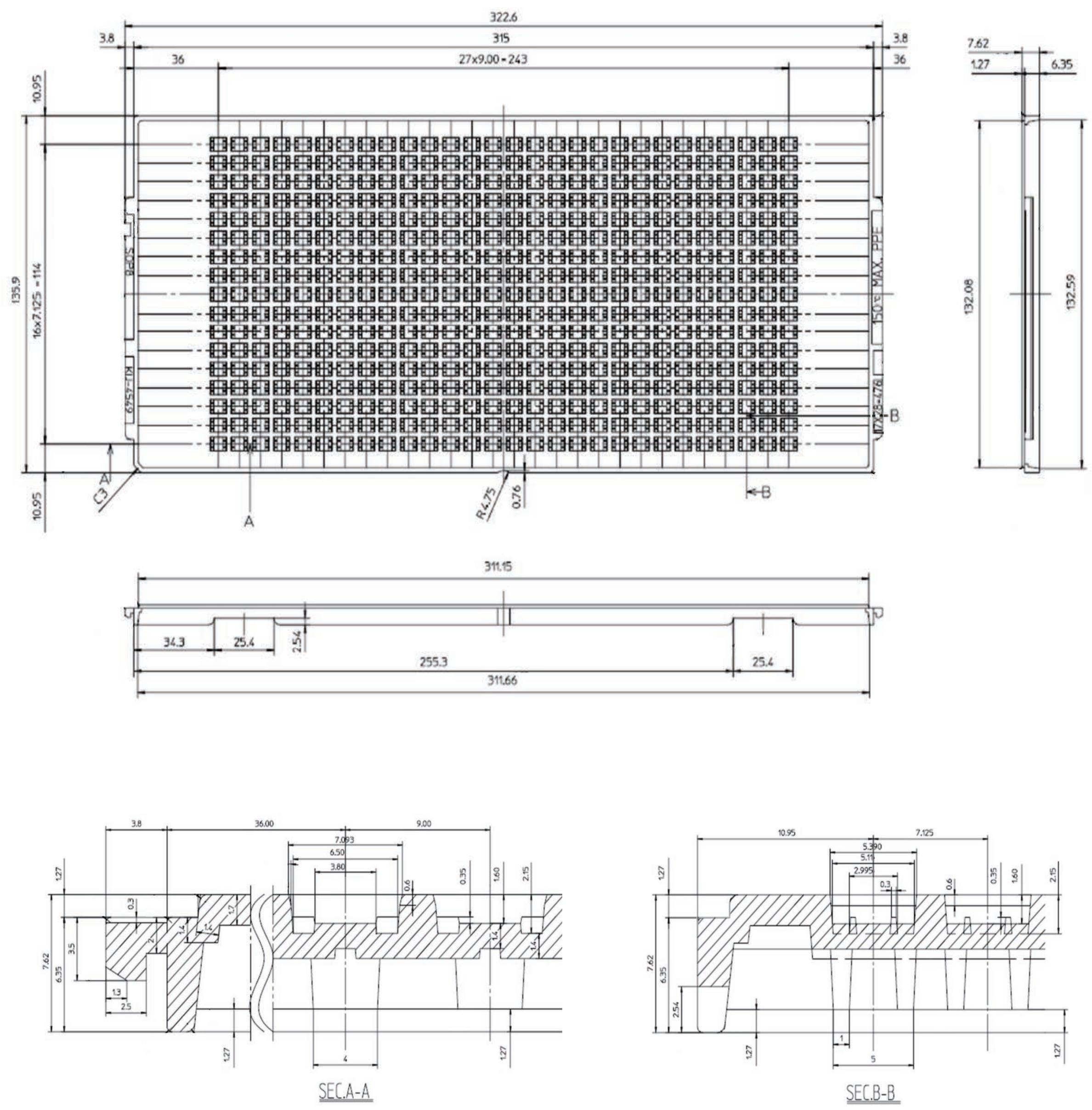
(Dimensions in mm)

3. Tray(MB85RC16PNF-G-AME2)

3.1 Tray Storage Capacity

Maximum storage capacity		
ICs/tray	ICs/inner box	ICs/outer box
476	4,760 (Max:10 trays/inner box)	19,040 (Max: 4 inner boxes/outer box)

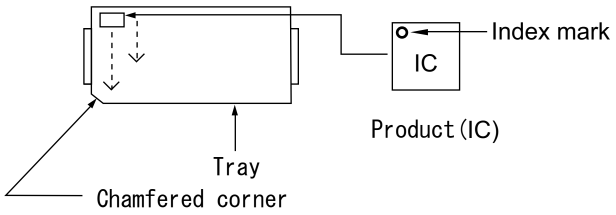
3.2 Tray Dimensions (JEDEC Standard)



(Dimensions in mm)

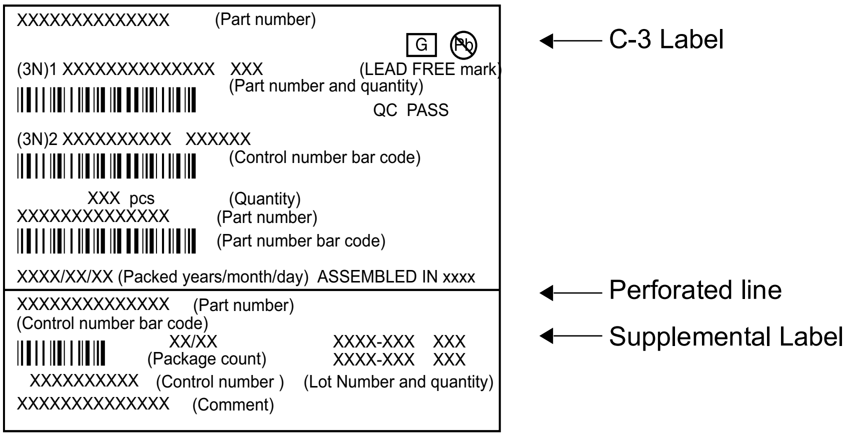
Heat proof temperature :150 °C Max.

3.3 IC Orientation



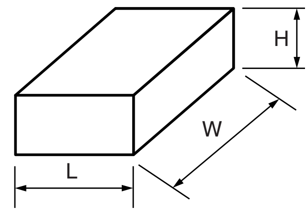
3.4 Product label indicators (an example)

Label on Inner box/Moisture Barrier Bag
[C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



3.5 Dimensions for Containers

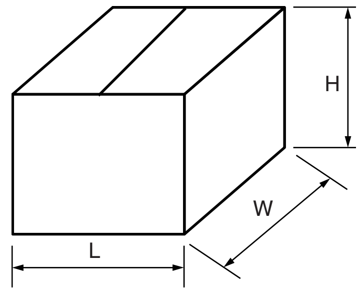
(1) Dimensions for inner box



L	W	H
165	360	75

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
355	385	195

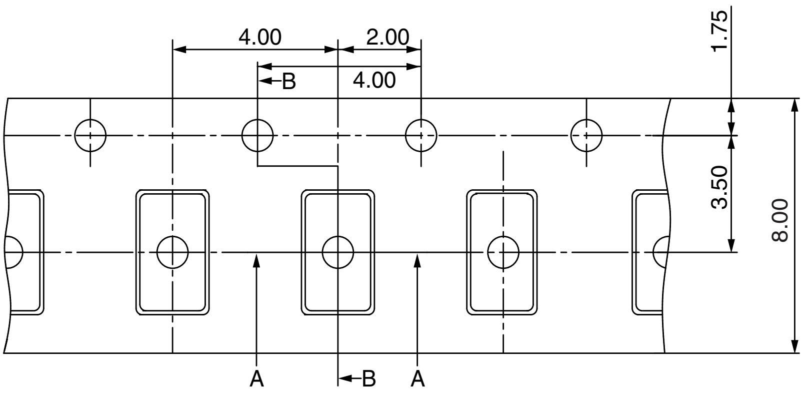
(Dimensions in mm)

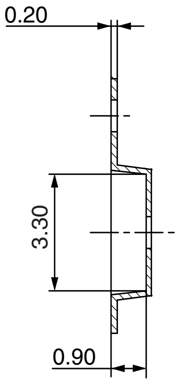
(2)MB85RC16PN-G-AMERE1

1. Emboss Tape (MB85RC16PN-G-AMERE1)

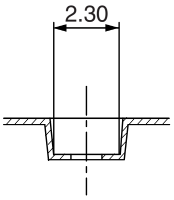
1.1 Tape Dimensions (not drawn to scale) (8-pin plastic SON)

Maximum storage capacity		
pcs/reel(ϕ254mm)	ICs/inner box	ICs/outer box
1500	1500 (1 pack/inner box)	9000 (6 inner boxes/outer box:Max.)





SEC.B-B

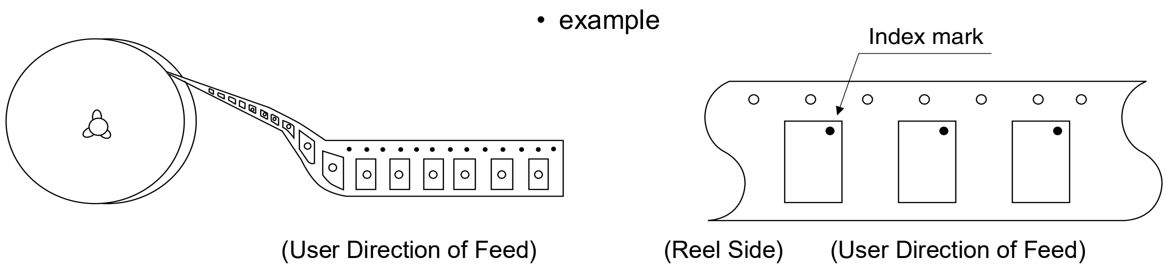


SEC.A-A

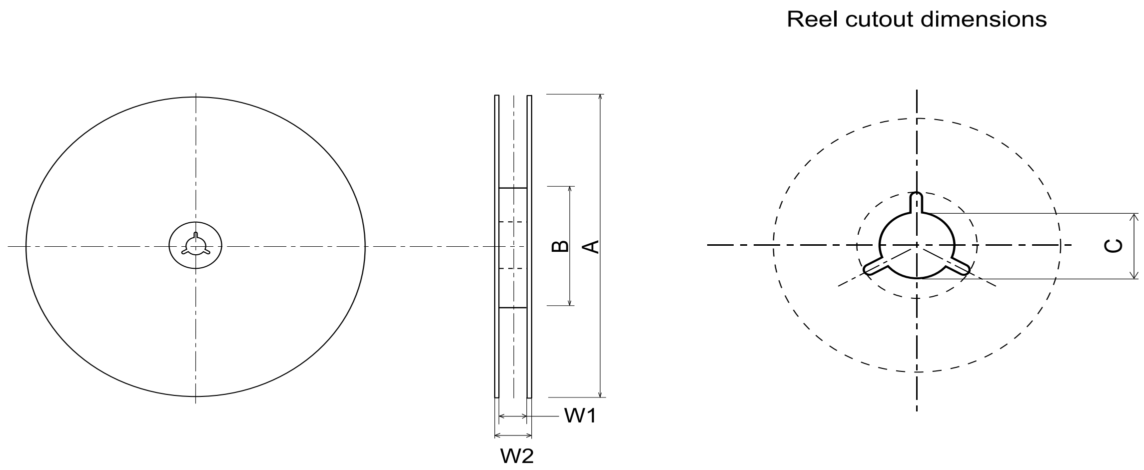
(Dimension in mm)

Heat proof temperature : No heat resistance.
Package should not be baked by using tape and reel.

1.2 IC orientation



1.3 Reel dimensions

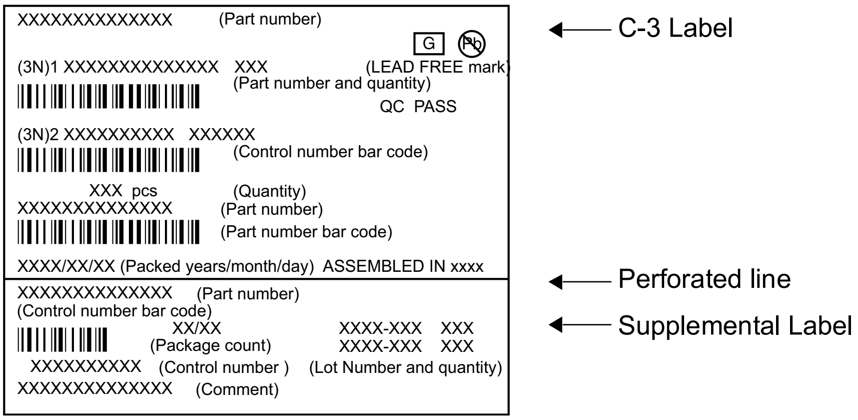


Dimensions in mm

tape width	A	B	C	W1	W2
8	254	100	13	9.5	13.5

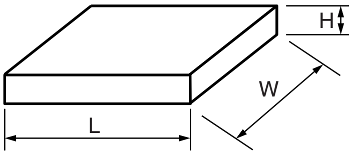
1.4 Product label indicators (an example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]


XXXXXXXXXXXXXX (Part number)
G Pb
(3N)1 XXXXXXXXXXXXXX XXX (LEAD FREE mark)
(Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX
(Control number bar code)
XXX pcs (Quantity)
XXXXXXXXXXXXXX (Part number)
(Part number bar code)
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx
XXXXXXXXXXXXXX (Part number)
(Control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (Control number) (Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)

1.5 Dimensions for Containers

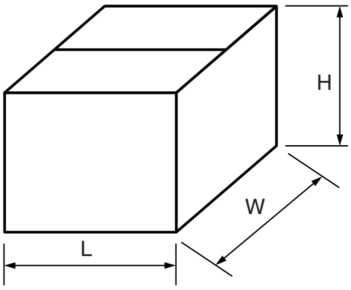
(1) Dimensions for inner box



L	W	H
265	**260**	**50**

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
565	270	180

(Dimensions in mm)

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
—	Overall	Following technical word is revised to more commonly used one. FRAM to FeRAM
18	ORDERING INFORMATION	Add MB85RC16PNF-G-AME2 and MB85RC16PNF-G-AMERE2.
21	MARKING	Add MB85RC16PNF-G-AME2 and MB85RC16PNF-G-AMERE2.
25	PACKING INFORMATION(1) 2	Add new part number, MB85RC16PNF-G-AMERE2.
28	PACKING INFORMATION(1) 3	Add “Tray” for new part number, MB85RC16PNF-G-AME2.
31	PACKING INFORMATION(2)	Add existing part number, MB85RC16PN-G-AMERE1.

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